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FIR Filter Design using Finfets at 22nm Technology

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Abstract: ***Finite Impulse Response (FIR) filters are the most significantdevice in digital signal processing.In many Digital Signal Processing applications like wireless communication, image and video processing FIR filters are used.Digital FIR filters primarily consists of multipliers, adders and delay elements. Area, power optimization and speed are the key design metrics of FiniteImpulse Response filter.As more electronic devices are battery operated, power consumption constraint becomes a major issue. Multipliers are the core of FIR filters. They consume a lot of energy and are generally complex circuits. With each new process technologies, the short channel effects limit the performance of FIR filters at nano regime. Various architectures have been proposed to enhance the performance of FIR filter. In this paper, FIR filter is designed using FINFETs at 22nm technology using Hspice software.***

Keywords: FIR, SCE, FINFETs

I. INTRODUCTION

In digital signal processing applications,especially in image and video processing, filtering is considered as the fundamental step. Basically the filters are classified in to two categories. They are Analog and Digital filters. To remove undesirable components of a signal, filters are used. Generally to get spectral shaping i.e., equalization, signal detection digital filters are used. In order to design digital filters the basic components needed are adders, multipliers and shift registers. Based on the architecture complexity, speed and power consumption are different [1]. A digital filter is basically a frequency selective network, which selects only a certain portion of input signal and rejects remaining portion of the signal. Digital filters have better signal to noise (S/N) ratio than analog filters. Digital filter allows sequence of input samples through it computes them and produces different output samples.The digital filters are categorized into two. They are FIR and IIR digital filters. The major disadvantage of IIR digital filter is that the closed-form IIR designs arerestricted to low pass, band pass, and high pass filters etc. Secondly FIR digital filters have precise linear phase [2, 3]. Due to stability and linear-phase property, Digital Signal Processing (DSP) applications make use of FIR filters extensively [4]. The key design metrics in fabrication of high performance DSP systems are low power consumption and less area.Now-a-days, FIR filters are designed to achieve either high speed or low power or less area.

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Adders, multipliers and Delay element are the key components used in designing FIR filter.

II. EXISTING SYSTEM

The conventional structure of Finite Impulse Response filter is shown belowin Figure1. FIR filter designinvolves three basic building blocks: Addition, Multiplication, Signal delay. The response of FIR filter is expressed as

$$y(n) = \sum_{k=0}^{N-1} b_k x(n-k) \quad (1)$$

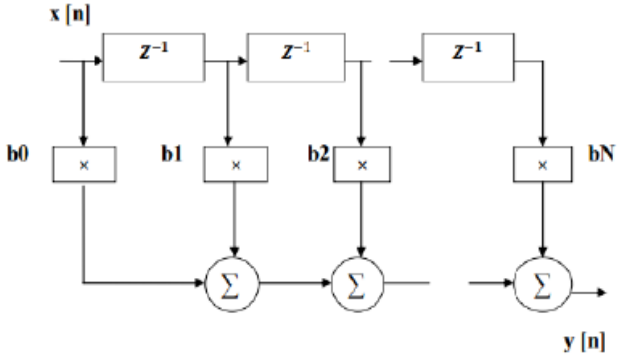


Fig.1 conventional FIR filter Block diagram

Where N signifies filter order, y [n] is the outputsignal and bk signifies filter coefficients. Applied input signal is x[n] and x [n - k] terms are referred as tapped delay lines. In the conventional FIR design, multiplier block performs multiplication by generating partial products. If the multiplier digit is a 1, the multiplicand is simply copied down and represents the product. If the multiplier digit is a 0 the product is also 0. Therefore the area and delay will increase which affects the FIR filter performance.

III. PROPOSED METHOD

To extend MOSFET scaling beyond 45nm for high performance and low power applications, various device structures has been developed based on Silicon-On-Insulator technology. For high performance microprocessor applications partially depleted (PD) SOI technology is emerged. Later, ultra-thin-bodyfully depleted (FD) SOI and the non-planar FinFET devicestructures emerged as upcoming technologies..

To overcome Short channel effects in MOSFET at nano regime, Chenming Hu developed FINFET transistor at the University of California at Berkeley FinFET is termed as Fin-Field-Effect-Transistor. Today's micro-processors are designed with FINFET transistors due to its non-planar structure. Earlier, designs were processed on SOI (silicon on insulator) substrate.

However, in FinFETs,a thin silicon structure shaped like fin called gate electrode is made by creating a channel above the insulator. Due to this structure, multiple gates can be created to control the transistor.

This non planar structure enhances further scaling thereby extends Moore's law.

This structure enables manufacturers to design electronic circuits with small sizes, operate at very high speeds and also consumes very less power.Now a days,FINFET devices have been used in designing digital and analog circuit designs to get good performance.

Fig.2 shows the structure of a FinFET. The FinFET structure has a uniform front and back metal gate which are attached together enclosing the conducting channel. This structure gives way to better gate control over the channel. The flow of electrons from source to drain via conducting channel is perpendicular to the wafer plane and the current flows parallel to the wafer plane, therefore forming a quasi –planar device [6].

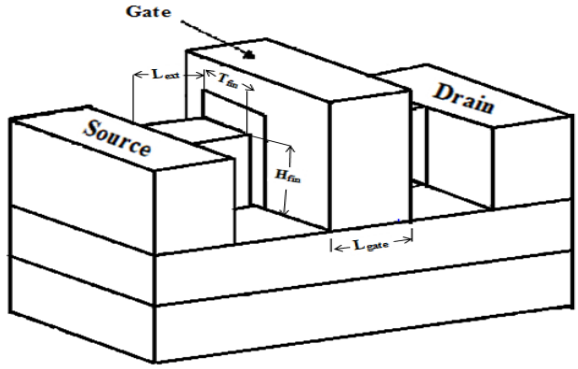


Fig.2 Structure of FinFET

The key feature in a FinFET is the formation of ultra-thin Silicon (Si) fins which forms the transistor channel to reduce the short channel effects. A FinFET can have multiple fins as per the process design. Multiple fins are usually used to achieve larger channel width. The dimension of this non-planar device affects the performance in terms of power dissipation and delay.

Channel effective length $L_{eff} = L_{gate} + 2\times L_{ext}$(2)

Channel effective width $W = T_{fin} + 2\times H_{fin}$ (3)

Where H_{fin} and $T_{fin}$are height and thickness of fin.L_{gate} is length of the gate,L_{ext} is extended source or drain region as explained in Figure 1. Fin width (T_{fin}) plays a key role in controlling the short channel effects effectively. Therefore $T_{fin} \sim L_{gate}/2$ is followed [7].

InFinFETconstruction, the charge carriers willtravel from source to drainregions through the conducting channel formed by an ultra-thin Silicon fin. The conducting channel is surrounded by the gate terminal where the input voltages are provided. This prevents the flow of charge carriers through the device even in off state. Thus controls leakage current flow. Sometimes, the conducting channel formed by a single fin breaks down due to increase in rate of charge carrier flow resulting in cease of charge carrier flow from source to drain.

FinFET is a double-gate MOSFET, however to keep the short channel effect in MOSFET in control, the number of gates are increased forming multi-gate field effect transistor (MuGFET). Multi gate FET devices are considered as an alternative for MOSFET [8]. This allows better drive current and channel control. Among all multi-gate field effect transistors, the FinFET is widely accepted device.

FinFETs have various logic design styles. FINFET operates in various modes

A. Short Gate (SG) Mode:

In this mode, the front gate and the back gate are joined together to form single gate terminal. The drive strength of this type of structure is good and also provide low leakage currents.

B. Independent Gate (IG) Mode:

Here, in this mode, input voltages are fed to front and back gate terminals independently. The delay is more with these arrangements compared to conventional CMOS.

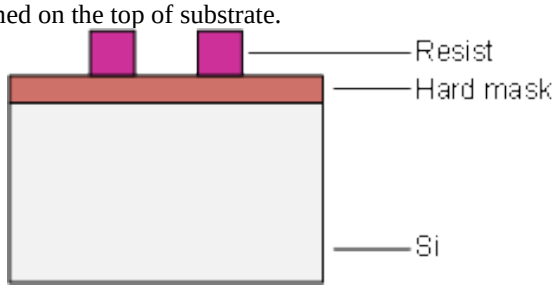
C. Hybrid Gate (IG/LP) Mode:

In the hybrid mode, both Independent gate mode and Low power modes are employed. Due to its combination, it includes advantages of both the modes. Therefore making the mode more efficient. As the Hybrid mode is designed, the number of transistor used to make the circuit are less in number.

Fabrication steps for constructing bulk silicon-based FinFET are

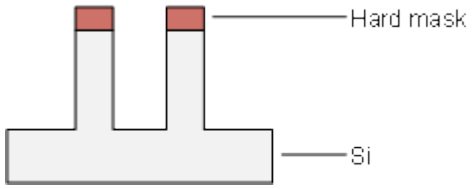
1. Substrate

FinFETstructure is formed by using a lightly doped p-type substrate with silicon nitride on its top. A resist layer is formed on the top of substrate.



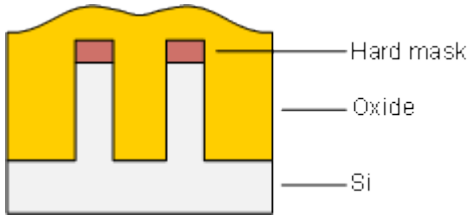
2. Etching of Fin

By using highly anisotropic etching process the fins are modeled. Here, etching process if performed based on timing due to the absence of stop layer on silicon wafer as inexists in Silicon OnInsulator. In 22 nm process technology, the width of the fins is set in between 10 to 15 nm and the height of fins is set to twice that or more.



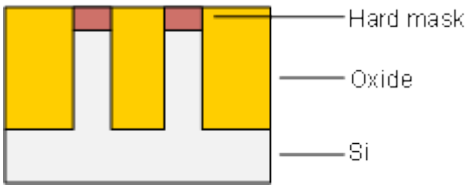
3. Oxide layer Deposition

To isolate the fins from one another, a high aspect ratiodeposition of oxide layer is needed.



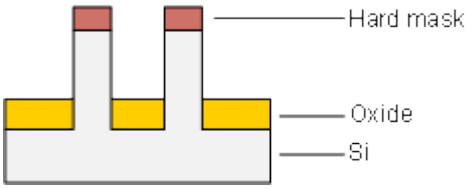
4. Planarization

By using chemical mechanical polishing, the oxide layer is planarized. This mask acts as a stop layer.



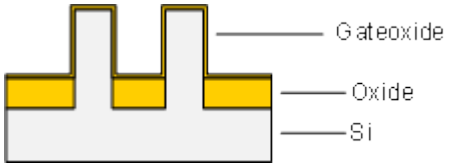
5. Recess etch

Lateral isolation of the fins is done by using another etching process in order to break oxide film.



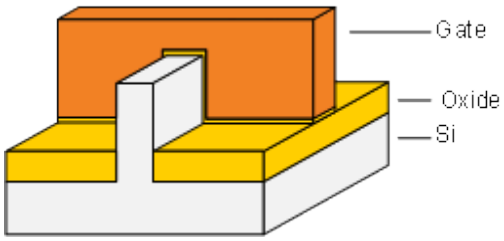
6. Gate oxide

Gate oxide layer is patterned on the top of the fins by using thermal oxidation in order to detach the channel from the gate electrode.At the bottom of fins, a high-dose angled implant is created to separate the fins that are stillassociated underneath the oxide layer.

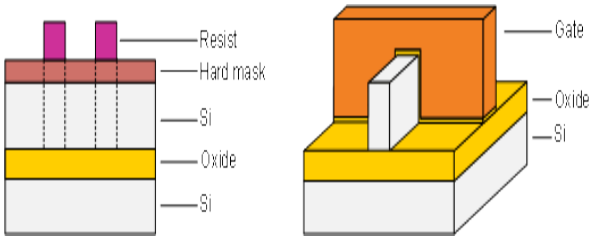


7. Deposition of the gate

On the upperside of the fins, a highly doped n+ poly layer is deposited to surround three gates around the channel.Twogate terminals are formed on either side of the fin, and third gate above the fin.



On the top of the channel, a nitride layer is deposited to influence the top gate.



IV. SIMULATION RESULTS

To enhance performance of FIR filters, the blocks of FIR are designed using FINFET transistors and simulated using Hspice software at 22nm technology node. The simulated results are shown below.

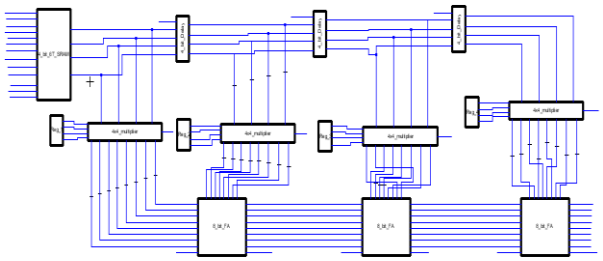


Fig.3.Complete Schematic of FIR filter

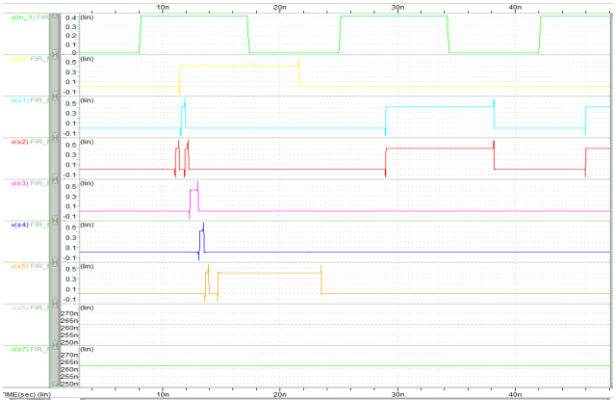


Fig.4.Response of FIR filter

Table.1 Tabulated Results for FIR Filter

Design	*Area (um^2)*	*Power*	*Leakage current*	*Delay*
7T - FIR filter design	1700.4	0.42x450u = 189uW	0.42x20 = 8.4u	0.2ns
6T - FIR filter design	1699.2	0.42*400u = 168uW	0.42*19u = 7.98u	0.1ns

V. CONCLUSION

In wireless communications, image processing and video processing applications, FIR filters are widely used. Power consumption, Area occupied and speed are the key design metrics fordigital circuits in high end processors. With rapid increase in battery operated devices, power consumption and speedconstraints become significant.For process technologies beyond 45nm, the SCEs affect the system performance. Since FINFETs offer better performance and low power than MOSFETs at nano regime, Here FIR filter is designed using FINFET transistor at 22nm technology using Hspice software.Simulation results illustrate that, FINFETs offer good performance at nano scale.

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