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Application of PODEM Algorithm for Fault Detection and Location in FinFet based Combinational VLSI Circuits

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Abstract*: *FinFet transistors are used in major semiconductor organizations and a significant role is played by it in developing the silicon industries. Due to few embedded memories and other circuit issues the transistors have specific faults in manufacturing, designing of the circuit etc. This paper presents an advanced test algorithm to diagnose those faults. The circuit with different gates is designed to identify the places having faults. In addition, different algorithms such as PODEM (Path Oriented Decision Making algorithms) are used to find the fault detection and location. The Furthermore, more complicated circuits are analyzed for fault detection with different approach. In this research work Combinational Circuits are designed using 20nm/32nm technology nodes in LT Spice environment and PODEM Algorithm is implemented which is developed in MATLAB, to detect and identify fault location and sensitive test vector to detect fault in the circuit and results are presented..

Keywords: Fin Fet transistors, Fault analysis, Transfer characteristics. , PODEM Algorithm, Fault Diagnosis, Fault Detection.

I. INTRODUCTION

The MOS transistor models are highly complex as the dimensions of devices are decreasing day by day. The model Parameters which is required for the circuit simulations needs to be extracted successfully. Alternate use of MOSFETs is the circuits involving the FinFet which is being investigated. The gate control over the channel is better when compared to MOSFETs[1].FinFETs are defined as the circuits with the shape of fins and is perpendicular to the structure of wafer in which the current is transferred. The existing fin will be sandwiched in-between front as well as back gates. **(Ref: Fig 1)** In order to suppress short channel effect, the structures of FinFETs are very thin[2]. Fins are compact and sophisticated such that its size is less than the channel length. The traditional use of the planar bulk equipment of sub 25 nm with short channel behaviour, reduced leakage current and excellent fabrication process is replaced by the double gate FinFet transistors which remain considered as the worst substitute. By adopting simple manufacturing process and having goodcompatibility with planar MOSFET, FinFet is considered as one of the most feasible multi-gate devices[3].

Numerous The conventional MOSFET is used for the scaling of power which is an issue due to short channel effect [4].

There are numerous types of fault models available for FinFETS[5] .There are few problems associated with the design of FinFet circuits in various applications. At various levels of abstraction, fault modelling for the planar single gate

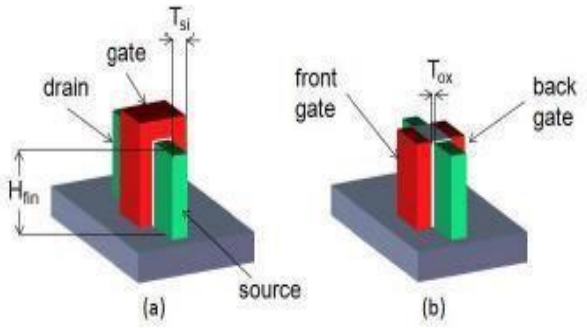

Figure1.A) Shorted gate B) Independent gate FinFETs.

CMOS is researched extensively[6]. Considering an example of bridging, stuck-open faults and stuck at delay faults are the broadly utilized fault models in CMOS. Several defects such as resistive shorts and open are found because of the improvements in the technology. The technology advancement also leads to the process variability of manufactured circuits. The process variability makes the interconnected parameters modelled as random variables. The uncertainty is captured by the random variables by the process variability, change in the environment conditions such as temperature, voltage etc.

II. RELATED WORK AND LITERATURE SURVEY

1. The specific faults in FinFet circuits with a new strategy are presented [8]. Further the fault modelling is performed and besides that, test algorithm which is novel is proposed for synthesis. The validation isperformed on the other FinFet based embedded technologies. Faults specific to the FinFETs are identified.

2. The work is based on the model of FAST fault and is proposed on behalf of the insignificant delay faults by the cross-gate defects in FinFET[9].

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The test patterns are generated as well as selected using FAST ATPG, test selection and fault simulation. The comparison is made between the FAST SDQL and FAST coverage and the pattern sets which are obtained are 29% and 4% respectively.

3. The problems associated with the fault diagnosis are overcome by an improved partial least square approach (IPLS)[10]. The IPLS helps in decomposing the process variables with the key performance indicator related part. Fault diagnosis information is obtained by the test statistics which are designed and the desired performance of the systems is presented. The proposed approach helps in diagnosing KPI faults and also provides the high fault detection rate.

4. A new approach is presented to find the internal cell delay effects using the analog simulation-based fault models [11].

5. All the defects present in the FinFet circuits are modelled by the CMOS fault models. Mixed-mode Centaurs TCAD device is used for the simulation of the problems which are present in the circuit and shows that the faults overlap in a planar MOSFET and FINFET[12]. New faults are required to capture the behaviour of the logic gates.

6. The sequential test generation algorithm which is more effective for the sequential circuits is implemented[13]. The standard PODEM algorithm using C ++ which is fully tested using combinational circuits is proposed. The results show that test patterns on behalf of line stuck-at faults may be generated for the circuits.

7. To overcome the inefficiency PODEM is introduced[14]. This algorithm is employed to generate automatic test patterns and also expanded the binary decision tree around primary input variables. This algorithm also has sub routine to check the existence of D frontier. Backtracking is also explained in this work using PODEM algorithm. The defect level on behalf of faults is determined by means of a Function of Fault Coverage as well as production. With the help of the definition, the number of stuck-at-faults that are tested as m and divided with the entire amount of stuck-at-faults n is called as the fault coverage T. The defect level equation as well as the fault coverage is interrelated proportionally with one another which is the main issue.

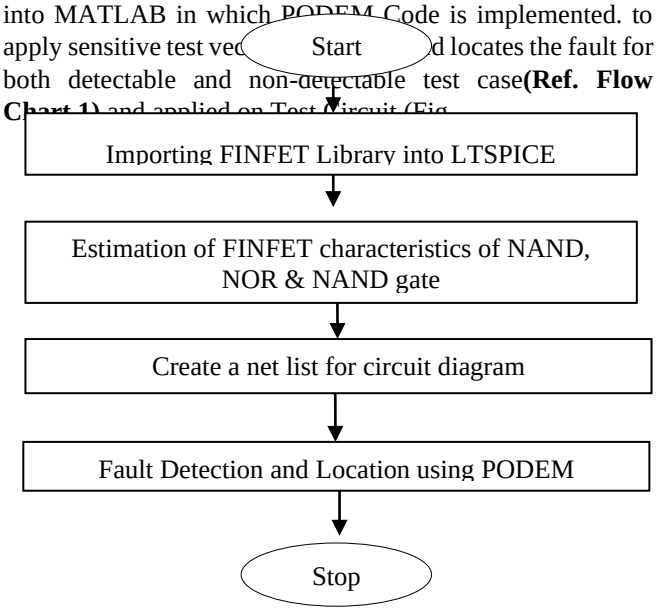
8. This paper[13] integrates various algorithms as well as methods regarding the test generation within a unified system that proposed tests on behalf of un-partitioned LSSD logic structures of up to 50,000 logic gates. This paper presents the designing concept in creating the unified system by means of results achieved upon huge logical structures. The VLSI LSSD logic structures achieve the feasible test generation ability as shown in the outcomes of the test generation system.

9. The redundant circuit logic is identified and the implementations of various circuits are compared by generating the circuit test patterns by Automatic-test-pattern generation algorithms. Operative test is impractical for larger circuits and E-beam testing was very expensive. To overcome this inefficiency PODEM[16] was introduced PODEM expanded the binary decision tree around primary input variables only, thus accelerating the algorithm. PODEM algorithm had a subroutine to check the existence of D-frontier. If not, PODEM backtracks immediately, thus speeding up the process. Backtracking is an important method introduced by Goel[13] in PODEM.

10. A deficiency model which is used within the computerized circuits[17] is called as Single stuck line. A line or a hub that is stuck at logical high or low within the computerized circuit is expected by the model. Whenever a line is stuck, it is known as fault. The reliability is enhanced by weighing the required overhead and the fault tolerance is achieved by introducing the redundancy within the digital circuits. A novel design is achieved that simulates the fault on behalf of a digital combinational circuit and it is constructed from 10 gates and 3 inputs using 1 output. C language is implemented to write the code and outcomes of the single stuck at all faults are presented in detail. Using 10 gates, 3 inputs and 1 output, the implementation of deductive fault simulator is done on behalf of the digital circuit and moreover it implemented and tested.

III. PROPOSED METHODOLOGY

The proposed method used for fault detection and fault location is **path-oriented decision-making algorithm(PODEM).** The first step is effective testing and diagnosing of faults to be carried out in FinFet circuits. For this purpose, the designing of NAND, NOT, NOR gates are done in LTSPICE using FinFET Models(20nm/32nm) and then creating a net list for circuit diagram and later importing into MATLAB in which PODEM Code is implemented. to apply sensitive test ve d locates the fault for both detectable and non-detectable test case**(Ref. Flow Chart 1)** and applied on Test Circuit (Fig



3.1 Design of Gates

3.1.1 NAND GATE:

The design of NAND gate using FinFET models as shown in the below **figure. 2,** shows that V1, V2, V3 are considered as 1V. V1 and V2 are considered as input voltage and V3 is used as power supply to FinFET model. VTC curve and delay calculations is a plot of input vs output. The graph of the transfer curve needs to be plotted. The Vth and Vih VIL, VOH, VOL all these simulation parameters along with the noise margin high (NMH = |VOH - VIH |) as well as noise margins low (NML = |VIL - VOL|) are calculated and for NOR and NOT gates also results are given **(Ref.Table-1)**

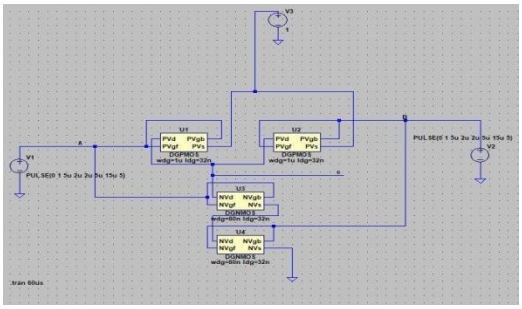


Fig 2. NAND gate design using FinFET library

After the design of the gates these gates are constructed together to find out the fault diagnosis (Refer Fig 3)

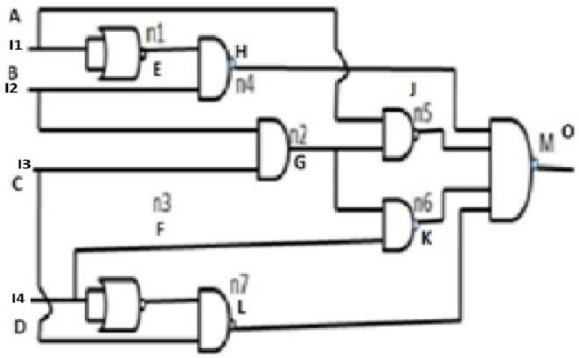


Figure3: Podem Algorithm Test Circuit

NAND GATE:

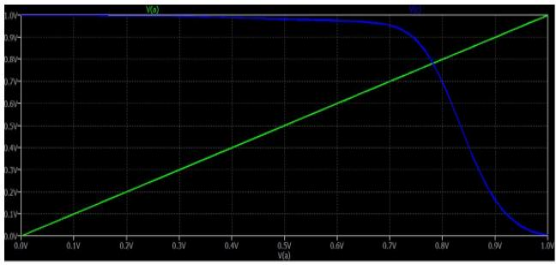


Fig 4: Transfer Characteristics curve f NAND gate.

From the above figure the parameters obtained are,

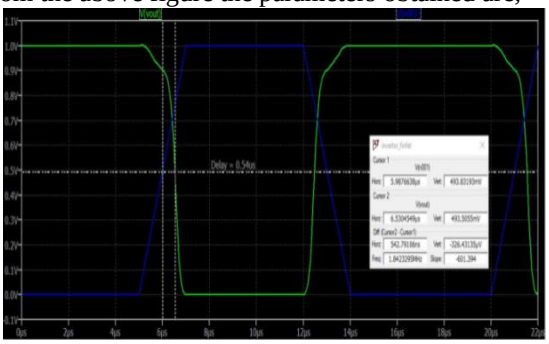


Fig 5: Delay Characteristics of NAND gate

The above fig shows the FinFET NAND gate's delay characteristics. The steady state values obtained are, High to low propagation delay (tpHL): Time is calculated which takes to fall from VOH to 50% Low to high propagation delay (tpLH): Time is calculated which takes to rise from 50% to VOL Propagation delay is calculated as (tp)= (tpHL + tpLH)/2 =0.67µS,

IV. GATE RESULTS

GATE Results are given below (Table-1)

[1] NAND	[2] NOR	[3] NOT
[4] V_{OH}= 0.9 V	[5] V_{OH}= 0.97 V	[6] V_{OH}= 0.8V
[7] V_{OL}= 1 V	[8] V_{OL}= 0.07 V	[9] V_{OL}= 0.66V
[10] NMH = |VOH - VIH| = 0.02 V	[11] NMH = |VOH - VIH| = 0.25 V	[12] NMH = |VOH - VIH| = 0.07 V
[13] NML = |VIL - VOL| = 0.64 V	[14] NML = |VIL - VOL| = 0.513V	[15] NML = |VIL - VOL| = 0.56 V
[16] Propagation Delay (tp): (tpHL + tpLH)/2 = 0.67 μs.	[17] Propagation Delay (tp): (tpHL + tpLH)/2 = 0.04 μs.	[18] Propagation Delay (tp):(tpHL + tpLH)/2 = 0.54 μs.

4.1 .PODEM (Path-Oriented Decision Making) ALGORITHM IMPLIMENTATION

An Automatic Test Pattern Generation (ATPG) algorithm is called as **PODEM** (Path-Oriented Decision Making). The aim of this project is to implement the PODEM algorithm for generating test vectors on behalf of a given fault. Given a circuit and a fault location this algorithm will tell us whether the fault can be detected and a combination of input values which can detect the fault. Whenever one exists, the output resembles a test otherwise it resembles that it is an untestable fault.

Assumptions:

1. Single stuck-at fault.
2. Written code assuming only 4 types of gates in net list but can be easily extended to other type of gates.

4.2 Input output descriptions:

Net list. Txt is the input file having description of nodes in spice net list format. The net list

We used in worked out example:

not1 n1 in1 and2_1 n2 in2 in3 not2 n3 in4 nand2_1 n4 in2 n1 nand2_2 n5 in1 n2 nand2_3 n6 n2 in4 nand2_4 n7 n3 in3 nand4_1 out1 n4 n5 n6 n7

in1, in2, in3 and in4 are the primary inputs. Out1 is the primary output. Our code can run for any such spice net list (for any number of inputs and any number of outputs)

Fault Location is the node where fault is to be checked, values should be taken from the net list files e.g. n1, n4. Fault Value is the complementary value of the stuck at fault.

"Fault is detected, Input vectors are:" will be the output in case given fault can be sensitized and propagated. "Fault is not detectable" will the output if either fault cannot be sensitized or cannot be propagated or both.

NCV = [1, 0, 1, 0, 1,-5,-5, 1] matrix for non-controlling value for each gate type

4.2.1PODEM (Path-Oriented Decision Making)

PODEM is an Automatic Test pattern (ATPG) Algorithm and it works in two major steps:

1. Sensitize the fault
2. Fault propagation

In the first step, appropriate PI (primary inputs) test are evaluated which excites the fault, that is, causes the complementary value to appear at the fault site

If this is found, then the circuit should be able to propagate the fault, for it to be detectable. In the second step, nodes that are connected to the output gate are assigned non controlling values. One sample circuit is chosen for verification purposes. Various subroutines of the PODEM algorithm are individually verified and explained in the below. Generic steps followed in algorithm:

1. Apply fault excitation conditions.
2. Implement the previous assignment effects.
3. Justify the remained unjustified lines whenever, one or more primary outputs are reached by the fault symptoms. In case that the justification is failed, back trace and go to Step 2.

4 Perform the resulting implications and go to step 2.

6. Once back tracing is completed, to propagate the fault, assign non-controlling values to nodes at output gate (by backtracking and assigning PIs appropriately)

In step 6, we always select a primary input (specifically for PODEM Algorithm). The process in which a suitable primary input is identified and assigns a value to it is known as back trace. Back trace procedure is given with an objective of an internal line in addition to a desired value intended for it and a path backwards is traced in the circuit until an input is found in PODEM and moreover it proved as the most effective over the D-ALG since its search space is limited towards the circuit's Primary Inputs (PIs). However, a search space is present in a D-ALG which includes the entire nodes within the circuit as well as the PIs.

The major modules of the MATLAB code are:

- Podem
- Main Podem
- Read net list
- Convert net list
- Create device map
- Cnctd devices
- Objective
- Back trace
- Imply
- Type
- Type imply
- Gates
-

4.2.2 BRIEF FUNCTIONALITY OF EACH MODULE

1. Podem:

Global variable declaration. Input assignment and calling function Main Podem

.2. Main Podem:

Input net list by calling "read net list" and "convert net list" Sensitize the fault

1. There are three major functions used here - objective, back trace and imply. Given a Fault Location, Fault Value pair, it back traces, and evaluates and updates values at each node

Fault propagation

1. Non-controlling value (NCV) is found for each node connected to output node.

2. Objective is called to set each of these nodes to this value. If a set of PI s is found which give NCV values at each of these nodes, „Fault is detected" is displayed along with the set of PI s

3.3.3 Read net list and convert net list

These functions read the spice net list, store the input and output nodes in format: [Device ID, Gate Type, Output node, Input Nodes]

Device ID is a unique number assigned to each gate using node map function. Gate Type is a number assigned to a particular type of gate as follows: **(Ref: Table -2 &3)**

Table 2

Type of gate	Gate type	Type of gate	Gate type
NOT	1	NAND 2-input	5
OR 2-input	2	XOR 2-input	6
AND 2-input	3	XNOR 2-input	7
NOR 2-input	4	NAND 4- input	8

*Have used only 4 gates – not, and, Nand, Nand 4 in the code.

4 .objective:

Input to this function is a particular nG, nV where nV is the required value at the node nG. It calls back trace function and back traces this pair of (nG, nV) till a primary input is achieved and isPI flag is asserted. After each back trace operation, value of nG, nV is updated to the next value in stack G.

5 Back trace:

Function is called inside objective. Takes an input pair (nG, nV). In every row of net list it checks where this nG is an output node of a gate. For this row, according to type of gate and nV, it evaluates the values of inputs of that gate using "type" function. These values of inputs to the gate are stored in a stack G and stack V variable.

6. Type:

Used in backtracking. Takes a row of format device ID, gate type, output nodes values, and input nodes values. Checks the type of gate and calls appropriate gate function (say Nand out for gate type = 5 for Nand gate) and returns the row with updated input values.

7. Imply:

The main objective of this operation is performing one logic simulation proceeding from the circuit depending upon the primary Input values. The inputs are (PI, PI Value) obtained from the objective function. It searches for the gates in net list where PI node is an input and stores them in device connected array. Then it calls "imply device" function which operates as: It calls "type imply" function which evaluates the output node values. Also updates the node values array. This runs in a while loop which runs till all primary outputs are implied.

8. Type imply:

Similar to type function but it is used in imply. According to the type, corresponding gates are called. Difference here is that inputs are known and output is to be implied. The updated row is output from the function.

9. Gates:

NAND OUT:

Function for 2 input NAND gate. Inputs to this function are the two inputs and output of the row which is to be updated and g. g will be 0 for backtracking and g=1 for implying.

AND OUT:

Similar to nand out. Nand 4input:

Similar to nand out.

NOT_OUT:

Similar to nand out. Worked out examples:

We have worked out the algorithm on the following circuit. Codes in MATLAB and python are in the code-and-demo folder.

Example:

Net list: Alphabets are shown here just to facilitate understanding of below diagram not1 n1(E) in1(A)

and2_1 n2 (G) in2 (B) in3(C)

not2 n3 (F) in4 (D) nand2_1 n4 (H) in2 n1 nand2_2 n5 (J) n1 n2 nand2_3 n6 (K) n2 in4

nand2_4 n7 (L) n3 in3 nand4_1 out1 (M) n4 n5 n6 n7 using node map function all nodes of net list will be assigned a unique device ID as given **in Table-3**

Table 3for results

Device ID	Nodes from Figure	Node of net list
1	E	n1
2	A	in1
3	G	n2
4	B	in2
5	C	in3
6	F	n3
7	D	in4
8	H	n4
9	J	n5
10	K	n6
11	L	n7
12	M	out1

V. RESULTS AND DISCUSSIONS

After running MATLAB CODE on Test CIRCUIT

1. Fault at node K i.e. stuck-at-1=> V =0:

Step 1: Set objective (K, 0) and back trace (K, 0) which gives (G,1) and (D,1). D = 1 found by backtracking (till a primary input). Now call imply (D, 1)

D = 1 implies F = 0 implies L = 1 while other nodes are still unassigned

Step 2: Now check for value at fault location. It is still unassigned (value = -5), so continue with using the second option of back trace (K, 0). i.e. (G, 1)(as stored in stack earlier) . Back trace (G, 1) gives (B,1) and (C,1).

Imply with (B, 1) gives G = -5, K = -5

Step 3: Now imply with C = 1. => G =1, K=0. So fault is sensitized. Step 4: For propagation, back trace (J, 1) => A =0, E =1, H= 0.

Step 5: Since H=0, fault cannot be propagated. So no test exists. And fault is not detectable 2 Fault at node K, stuck-at-0 => V =1

Step 1: Set objective (K, 1). Back trace (K, 1) => D=0. Imply (D,0) will give F=1, K=1.Fault at K is sensitized

Step 2: To propagate the fault, back trace (H,1) => (E, 0) => (A,1) , (B,X)

Imply (A, 1) => no changes in node values.

Step 3: back trace (J, 1) => (G, 0) => (C ,0) imply(C,0) => (J,1),(L,1)

Step 4: Since J, L and H, all are set to Non-controlling value of Nand4. Fault can be propagated. Input Vector is (A, B, C, D) = (1, X, 0, 0)

Proposed test algorithm that provides better diagnosing of faults in FinFET circuits

for the given test circuit

5.1 PODEM ALGORITHM RESULT:

```
Fault Location n2
Fault Value 1

Fault is detectable

Primary Input values are:
Node in1    1
Node in2    1
Node in3    1
Node in4    x
Fault is detectable

Primary Input values are:
Node in1    1
Node in2    1
Node in3    1
Node in4    1
>>>
```

Figure6 : Fault value is Detectable

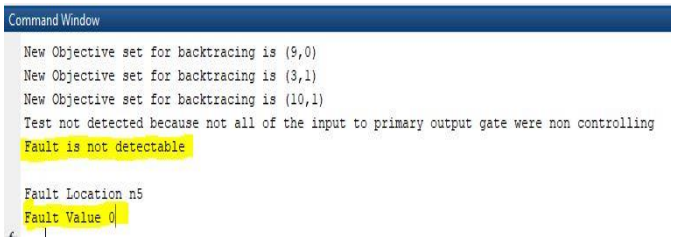


Figure7: Fault value is not Detectable

PODEM Algorithm for the Test Circuit (Ref: Fig 2) the fault is detected at node n4 (Device Id H) and Fault Value is 0, similarly for any given Fin FET based Circuit faults can be detected and location can be identified with sensitive Test Vector at the inputs Ref:Figsd 6 &7)

VI. CONCLUSION

In this paper, designing of NAND, NOR and NOT gates are done using FinFet model & each gate with logic outputs are verified as shown in graphs. The simulation results show that for each gate VTC curves has been plotted and delays, noise margin values (VTh, VIH, VIL, VOH, VOL, NMH, and NML) areobtained.

The circuit diagram is designed and faults are analyzed, detected and fault location is identified for the given circuit. Sensitive input Test Vectors are identified for both Fault detectable and not Detectable conditions (**Ref: 6 & 7**) By using PODEM algorithm, fault location and faults are obtained, best vector selection is found. Furthermore, In this Research work it is attempted application of PODEM Algorithm concept to detect and find fault location in advanced 20nm/32nm FinFET based Combinational Circuits for the first time and it is proved**.**

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K V B V Rayudu graduated from Institution of Electronics and telecommunication Engineers (IETE), New Delhi during Dec 1990 and obtained MS Centre Imarat (RCI), DRDO, Hyderabad as Scientist in R&QA activities of Missile Systems. Contributed significantly in Parts Management, Qualification, Testing, Failure Analysis, reliability Analysis & Screening Policy of Electronic Components & Systems for Aerospace Applications. Planned and Played Key role for ISO 9001:2000 Certification and Aerospace Quality Management System AS 9100:2009certification to RCI, Hyderabad. His Research Interests include VLSI Testing, VLSI Fault Simulation, Modelling & Diagnosis Reliability Analysis, Failure Analysis, Quality Management System Certifications applications of ANN, GA, SVM for optimization etc.

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Second Author profile which contains their education details, their publications, research work, membership, achievements, with photo that will be maximum 200-400 words.

Dr.Sriharirao Patri is working as Assoc Prof at NITWarangal in the dept.of ECE. His Research intrests include RFIC Design, VLSI Testing, Fault Diagnosis Analog/digital IC design, DSP Architecture, Analog LDO's. He has published 10 technical papers in Reputed international journals/Presented in Conferences. He has conducted various cour in VLSI area and guided 5PhD Students.