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Design and Interfacing of I2C Master with Register and LCD Slaves

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Abstract*: One of the foremost, well-liked, less sophisticated Serial communication standards, I2C; a bus protocol familiarly meant for the exchange of information among the peripherals residing on the constant circuit card, houses two-wires i.e., data and clock for supporting duplex communication between multiple masters and slaves do considered as prominent and efficient in Data transmission. The present work emphasizes on the I2C controller designed for interfacing with slaves, a simple control register of I2C switches/card where the data is written or scan from, subsequently, I2C core implementation on Spartan 3E FPGA, where one of its on-chip peripheral, in this case LCD treated as a slave for performing data transactions. The entire module is designed in Verilog HDL, functional checking is accomplished with the ISIM 10.0b simulator, followed by the design synthesis using Xilinx ISE14.4 tool

Keywords: Communication protocols, I2C Bus, I2C Switch, Peripheral interface, SoC, and FPGA.

I. INTRODUCTION

Although Communication Protocols are classified in to serial and parallel, parallel buses are constrained to certain applications that may not always meet an excellent trade-off between delay, power, cost and performance. Contrarily, serial buses come in to play and are utilized in on-board communications (IC's or SoC's) for data transfer among processors and dissimilar sub-system peripherals.

Serial communication protocols [4] SPI, UART, USB, IEE1394 which are operated with a single master uses multiplexing of information for forwarding of messages to service multiple peripherals, but in a regular SoC communication we find many peripherals conveying information with many other indeed a bus protocol that supports multi- master and slave is required, hence the I2C[9] comes in to play as a two-way serial bidirectional bus developed by Philips Semiconductors in the early 1980s formerly to connect a CPU with various peripheral chips in a TV-set. Figure 1 shows the I2C interconnect in typical embedded systems.

RS-232, RS-422, RS-485 [5] and SPI [3] which are Serial by virtue of its nature are employed for interfacing high speed with low-speed peripherals hold more no. of pins and are enormous in size,

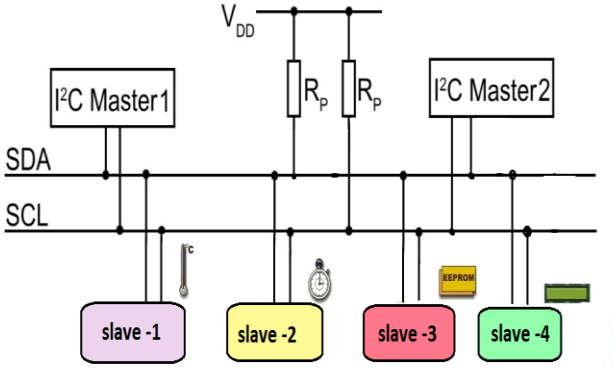

Fig 1: I2C bus with multi-master and slaves

But, it is known that the Evolution of VLSI design industry urges for miniaturization, to cope up with, all the inter subsystem logical blocks or intercommunication protocol modules yet to be scaled down from their bulky sophisticated adaptations for realizing effective IC or SoC's. It is also noticed that for the past few decades the physical size of IC has slashed, ultimately created a thirst for requiring less quantity of pin association and conciseness for serial data transfer schemes. Hence I2C (Inter-integrated-circuit) evolved that not solely simplifies the system level interconnect design however conjointly improves system performance since the transmission of digital data information is a lot of less prone to interference from environmental glitches and noise sources, throwing a challenge for the already available intercommunication version on FPGA Boards.

This article enlightens the I2C bus protocol with a revision on its characteristics and working principle, following with I2C bus master core designed in Verilog HDL [12] to interface with simple register memory cards/switches, consequently the hardware ASIC implementation [11] of the I2Cmaster bus controller on Spartan 3E FPGA [16] to master the LCD peripheral on the board where the master/controller sends commands and data to the concerned peripherals dedicated pins, for the effective functioning of the system, the on-chip modules need to be in sync with each other by sharing resources with zero conflicts.

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II. FEATURES OF I2C

I2C which is most robust, sustainable and easily emulated is assorted with peripheral devices, Compatible with a numerous processor cores (micro 8,16,32 bits) that houses I^2C ports in its architectures is a low to medium speed bus protocol

I2C specialized at collision detection and arbitration [13] provides work for two lines/wires----.

SDA: Transmission of any digital data takes place through this line.

SCL: A clock line that is accountable for monitoring and synchronizing with data information of SDA.

I2C bus Serial communication occurs in four phases [1]

A. START generation:

A high-to-low transition on the SDA line whereas the SCL is high defines a START condition.

B. Slave Address Transfer:

Succeeding with the START signal is the slave address, a concatenation of seven-bit calling addresses followed by RW bit. The RW bit signifies data transfer direction, (R/W=0, signifies write, else read). The slave acknowledges by a bit at the 9th SCL clock cycle by making SDA to low once it is ready for a transaction and if its address matches with the master as shown in figure 2.

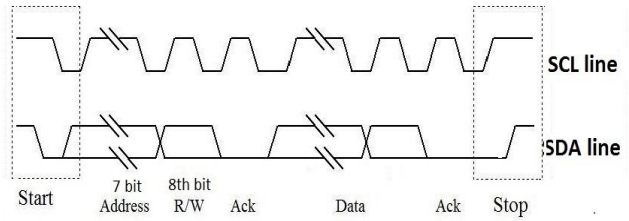

Fig 2: Data flow in I2C Bus

C. Data Transfer:

Each data bit is transferred by every clock pulse of the SCL. A byte i.e., eight bits transferred on the SDA line might be a peripheral address, register address or data written to or scan from a slave.

D. STOP generation:

A low-to-high transition on the SDA line whereas the SCL is high defines a STOP condition.

Any device, the master addresses is taken into account as a slave is recognized by a novel address whether or not it‘s a microcontroller, LCD driver, memory or keyboard interface that may operate as either a transmitter or receiver, reckoning on the requirement.

Throughout this group action, if RW =0/1; the master can become the master-transmitter/receiver and the slave can become the slave-receiver/transmitter. In the case of Read, at the end of each transaction byte the master-receiver can send an ACK (logic 0) to the transmitter letting the transmitter understand that it's prepared for accessing additional data. The receiver can follow this up with a STOP condition, the same ensures during Write operation.

The electrical attributes of the two wires in I2C Bus and detailed mechanism involved in working can be found in references [1].

III. CURRENT WORK & METHODOLOGY

The present work is organized into the protocol implementation part and application part, by taking aid of protocol a compatible interface is developed aiming for realizing applications. In certain applications, several cards hold devices as I2C slaves possess identical addresses; each card supervises some alarm system’s subsystem and operates LEDs for status indication. When an alarm is activated, an Interrupt is generated and is informed to the master. PCA9554 [6] type devices collect the Interrupt signals and send a “Card General Interrupt” to the master. As soon as the master reads/receives; immediately processes the alarm, by sending a reset signal to clear it. Since the cards are identical, it is required to de-conflict them and also to isolates the card that is not in admittance as presented in figure 3.

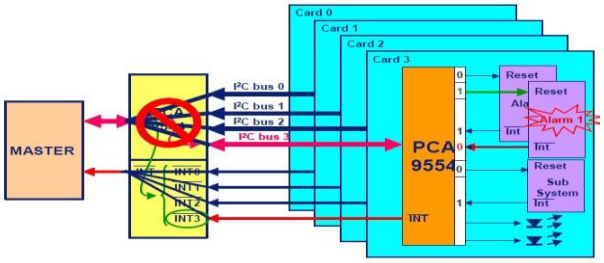

Fig 3: I2C Master accessing four different cards [9]

PCA9544 [7] resolves this conflict by creating 4 sub I2C busses that can be isolated, Collects the Interrupt from each card and disseminates a “General Interrupt” to the master

1. Master then interrogates the PCA9544 Interrupt status register to determine the card in the cause
2. Master then connects the related sub I2C channel in order to grill the PCA9554 by reading its Input register.

At last Master comes to know which card’s alarm got triggered to Process.

For certain scenarios, instead of dual 4 channel devices like PCA9544 [7], it is more compatible to use eight channels (bits) device i.e., PCA9548A an I2C switch with a reset capability acting as a perfect slave for I2C protocol; facilitates the I2C bus to split into sub-branches that are dynamic all the time and deactivates the one device if a particular branch hangs the bus, it reprograms the bus and detach the branch that is in fault, as its device address does not have a shift, once addressed.

The context is carried out in designing a Verilog code [12] for single I2C master controller interfacing with register switches and LCD serving as slave1&2 for the present framework; the proposed block diagram is illustrated in fig 4.

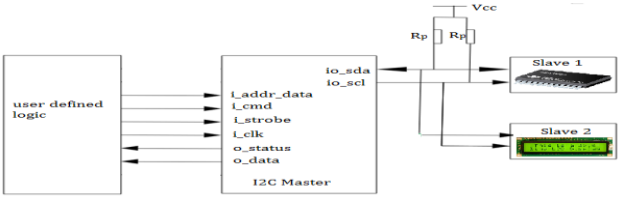

Fig 4: I2C Interfacing with slaves

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PCA9548A:

The PCA9548A [8] is an I2C multiplexer module that caps eight 8-channel (assuming 1byte register for each 8-bit channel/switch) devices or bidirectional translating switches whose addresses ranges from 0X70- 0X77 is controlled via the I2C-bus. Pin diagram is depicted in figure 5; upon selecting one of eight, a slave is selected as shown in Figure 6, in which any individual SCx/SDx channel or all eight channels of the addressed slave in switch can be selected, by configuring the programmable control register.

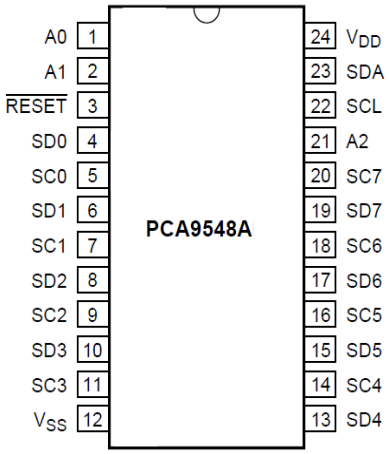

Fig 5: Pin diagram of PCA9548A [8]

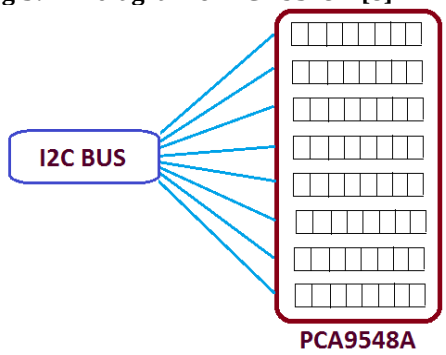

Fig 6: Addressing the target slave

Device address:

The bus master addresses the target by patterning the three address pins (A2, A1, A0) of the address register which are the selection inputs of the multiplexer as described in figure 7.

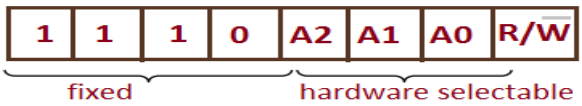

Fig 7: Address register of PCA9548A

Control register:

As soon as PCA9548A has been addressed, the bus master will send a byte to the PCA9548A, which will be stored in the control register depicted in figure 8. Each bit in register enables or disables a channel, thus master simply access the register information after the slave addressing, as shown below figure 9, 10.

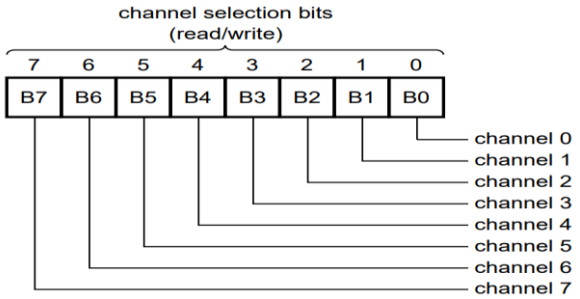

Fig 8: control register of PCA9548A [8]

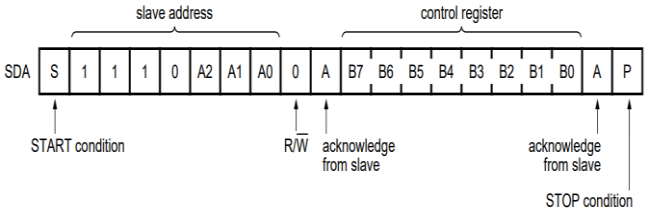

Fig 9: I2C initiates the switch for channel selection

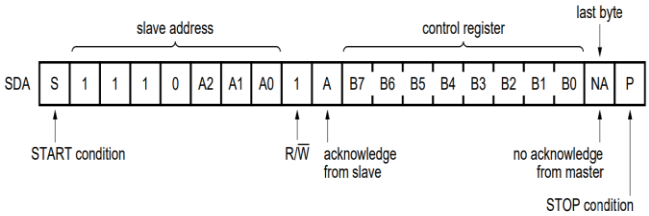

Fig 10: I2C accessing switch [8]

Applications that require for baud rate conversion [15] (processor to SPI device) I2C protocol is used. To access temperature at diverse locations-PCA9548A I2C Switch are employed [2], where digital temperature sensors are attached to channels: 0, 1, 2, 3. so on, to know the temperature at appropriate locations the corresponding channel is enabled/disabled. Similarly 8 OLEDs can be connected to the PCA9548A channels for displaying appliances. The I2C switch which is monitored by I2C controller also plays a vital role in Telecom Switching Equipment i.e., Servers, Routers etc.The 2-line, 16-character LCD screen embedded in Xilinx Spartan3E (500E) FPGA [16] development board kit is taken as slave2 which is programmed in Verilog HDL to interface with I2C Master. Once the FPGA mastered or programmed with I2C logic, it controls the LCD via the 4- bit data interfacing as shown in Figure 11. Although the LCD supports an 8-bit data interface, the Starter Kit board uses a 4-bit data interface to remain compatible with other Xilinx development features

Once I2C is implemented and mastered on FPGA, the LCD serves to display as many as ASCII characters. Operation and displaying any type of LCD Character according to requirement is being taken from LCD character Set of Xilinx UG230Spartan-3E FPGA Starter Kit Board User Guide

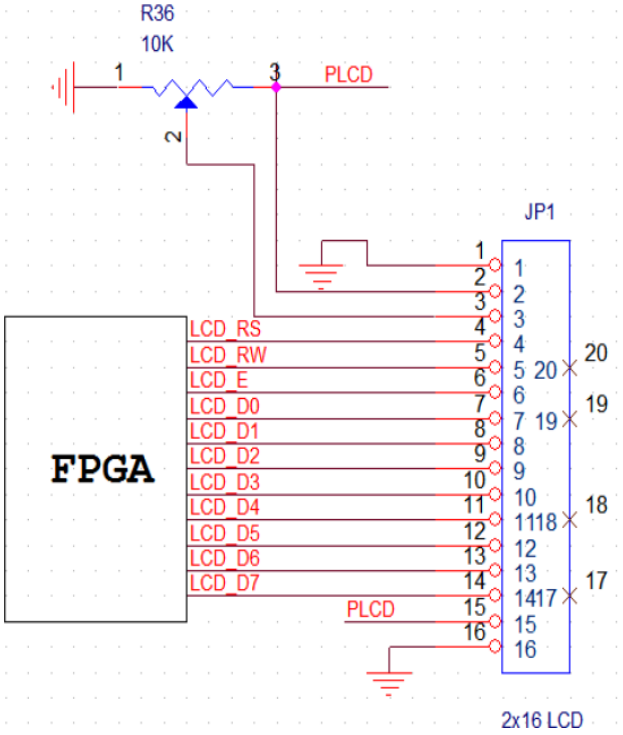

Fig 11: Interfacing diagram of I2C FPGA with LCD

Working Technique of LCD Character Set:

- For each of the characters that the LCD screen can display is located in the Character Generator ROM (CG ROM) that contains the font bitmap for the character.
- The character code stored in DD RAM for each character subsequently refers a position within the CG ROM.
- For example, a hexadecimal character code 0x54 stored in a DD RAM displays the character 'T'.
- The MSB nibble of 0x54 equates to DB [7:4] ="0101" binary and the LSB nibble equates to DB [3:0] = "0100" binary is "T".
- One byte command is divided into two 4-bit nibbles. Such that upper nibble is transferred first, followed by the lower nibble.
- English/Roman characters are stored in CG ROM at their equivalent ASCII code address as shown in figure 12.

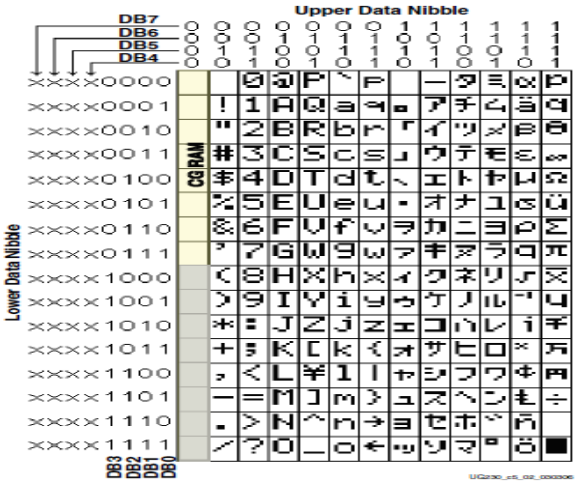

Fig 12: Characters at unique ASCII Address in CGROM [16]

IV. RESULTS AND DISCUSSIONS

The RTL schematic of I2C master interfacing with slave1 PCA9548A switch is portrayed in figure 13, simulation wave form is shown in figure 14

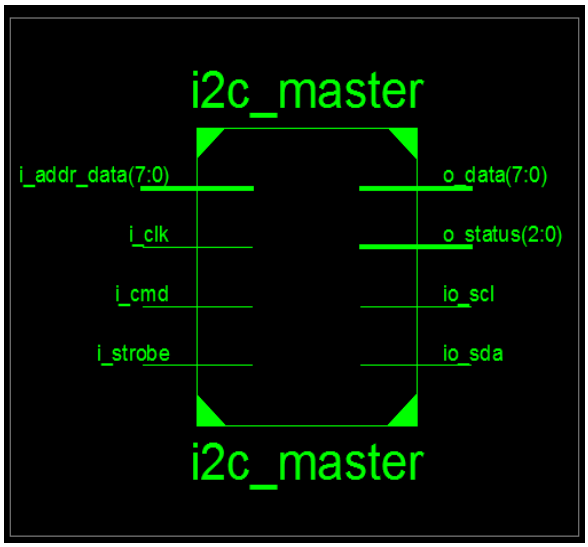

Fig 13: RTL Schematic of I2C master interfacing control register

The above simulation explains I2C Core is addressing 0X75H with write command and once it gets acknowledged, Master sends D4 Byte indicates CH- 2, 4, 6, 7 are enabled which may be attached to temperature sensor [14] or OLEDs or interfaced with any for a typical application. A number of clock cycles later if master desires to scan from configuration register of the switch, it addresses the same 75H slave and issues the R/W=1 , so that the no. of active channels can be scanned out.

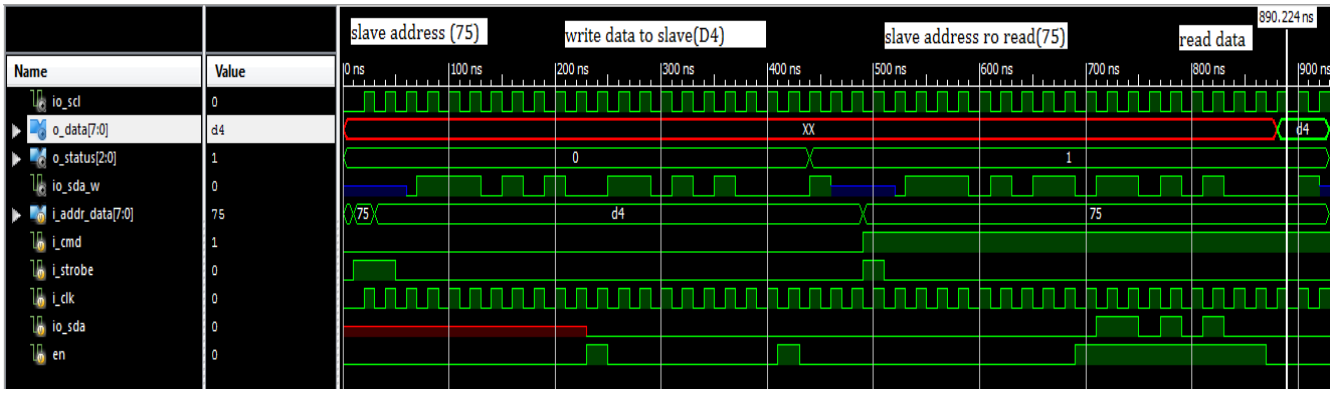

Fig 14: Simulation waveform of I2C accessing control registers for R/W operations

Fig 15: RTL Schematic of I2C master interfacing LCD

The RTL schematic of I2C master interfacing with slave2 i.e., is pictured in figure 15 and the hardware implementation of I2C on Spartan3E FPGA where the master I2c core writing some information (I2C PROJECT) on LCD screen is shown in figure 16.

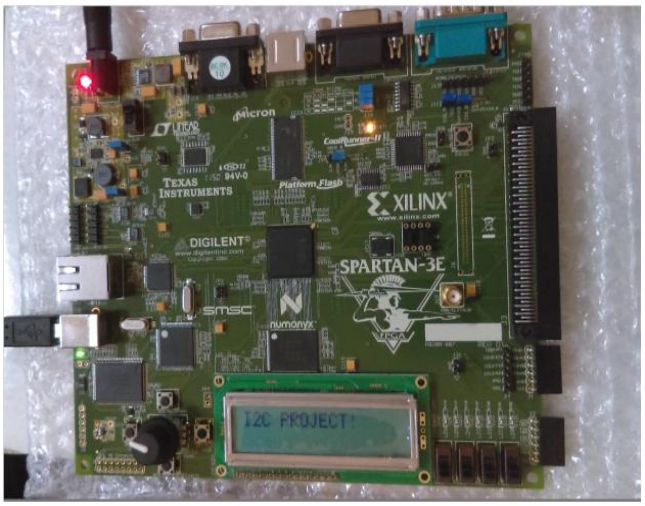

Fig 16: Hardware implementation of I2C on FPGA

V. CONCLUSION

The discussion started with serial communication protocols throwing light on I2C and its role in embedded boards, understanding the working mechanism of various I2C mastered peripherals, followed by designing an I2C bus controller which monitors and interfaces with the control register of PCA9548A i.e., I2C Switch admitted for conspicuous applications; Later the I2C Master core implementation on Spartan3E FPGA in which LCD a system on chip board peripheral has been treated as slave2 for performing effective read/write transactions. The Entire module is designed in Verilog HDL the functional correctness is verified in the ISIM simulator and carried out the design synthesis using Xilinx XST 14.4 tool.

VI. FUTURE SCOPE

As the number of devices assembled on a system board always increases to aim extra functionalities. The work can be enhanced for multi masters to aid large no of peripherals by providing a First in First out (FIFO) Queue for storing commands and data along with corresponding addresses of peripheral devices is considered as the scope for present work.

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