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THD Reduction in Multi-Level Inverters based on Multicarrier Pulse Width Modulation Technique

Kishore B, Senbakaraj, Periyasamy, Poongkabilan

Abstract ***Due to the advent of technology, electronic equipments are much more sensitive to harmonic and its analysis play an important role whereby reducing the distortion due to harmonics needs attention. To meet the requirements of the industries, harmonic free-high rating power sources are in high demand. Total Harmonic Distortion (THD) is an indicator of AC voltage source quality. In case of inverters, one such way to reduce THD would be the use of Pulse Width Modulation (PWM). The existing methods mainly use the low frequency pulse width modulation techniques for the switching. Control methods employing high frequency switching techniques held in controlling THD with proper application of filters. This paper analyses THD in multilevel inverters using multicarrier PWM technique with five pulse width modulation technique through MATLAB simulations. Finally, a comparison is done to find the less harmonic generated PWM method using fewer filters.***

Keywords: Harmonics, Multilevel Inverter, SPWM, Total Harmonic Distortion

I. INTRODUCTION

Practical industrial inverters are of non- sinusoidal in nature and are prone to harmonics. In case of low- power applications, voltage of quasi squared or pulse waveform is desired but high and moderate power applications warrant sinusoidal output waveforms with minimum distortion. Use of filters and certain techniques like PWM minimize the harmonics in the inverter's output. The former poses some demerits like size, cost etc. while the later helps in reducing the usage of filters

1. Total Harmonic Distortion

The total harmonic distortion is a common measure of signal harmonic level causing distortion at voltage or current level. It is referred as the ratio of total harmonics to that value at the fundamental frequency. It is usually given in percentage. There has been phenomenal increase of non-linear loads in the industries which may cause harmonics in the output. The non-linear loads imply loads which the applied voltage and current are not proportional to each other. These non-linear loads possess varying V-I characteristics.A marginal raise in voltage at times may result in doubling of current.

2. Multilevel Inverters

There is huge ever raising demand of electrical energy worldwide. This has led to the depletion of energy sources that are conventional in nature. Hence alternate sources are on the research track to support the extensive use of conventional sources. Renewable energy has now taken a crucial support for generating power. This type of energy has been on the front runner where inverters play a predominant role in converting power from DC to AC as demanded by loads. Small Scale Industries (SSI) and Utility applications mostly employ conventional three- or two-level inverters. Consequently, the concept of Multi-Level Inverters (MLIs) has served to a best alternate for high-power and medium power conversion systems. Generation of common mode voltage is a drawback faced by conventional dual inverters which are overcome by MLI technology [1]. Introduced in early 1975, the MLI topology has taken various variants till now. Owing to certain merits of MLIs such as immunity to EMI, better efficiency with lower switching loss and ability to operate at high voltages, these MLIs have taken the driver's seat in current industrial scenario. Besides, they are capable of meeting the ever raising power demand by offering enhanced power quality by the way of subsequent harmonic distortion minimization. It is possible to obtain a very good quality of staircase voltage (AC) from various connection including power-semiconductor switches. Operation with low switching frequency has made these inverters to be used for power conversion mechanisms.

MLIs find extensive applications in electric drive and vehicles, electric traction, renewable energy conversion etc. Less distorted output with lower harmonic content, capability to operate at both high and fundamental frequency PWM, less common-mode voltage, multiple states of switching etc are some of the important features of MLIs. Besides these merits, MLIs face some challenges in modulation and controlling schemes.

It is seen that dominant harmonics of lower order appear in the stepped-up output of the MLIs.

These challenges lead to fluctuation in voltage, malfunctioning and subsequent loss resulting in reduced power quality.

To overcome these challenges, an appropriate control method or scheme is needed and has to be implemented for MLI.

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Many researches have shown a solution of different diversified modulation strategies to control MLI effectively. It is inferred that enhancement in harmonic profiles and overall reduction in loss have major impact on the MLIs and these controlling methods are widely outlined in the literature works.

3. Switching Method

The two basic modes of control strategy that are followed widely are the fundamental and high- frequency switching methods. Better transient response is expected out of latter type namely conventional pulse width modulation (CPWM), sinusoidal PWM (SPWM) and space vector modulation (SVPWM). Various Carrier-based PWM techniques are efficiently and effectively introduced reducing the distortion and thereby lowering the interference. Carrier based PWM techniques generally, can be divided into: Phase Shifted PWM (PS-PWM) and Level-Shifted PWM (LS-PWM) technique. In the former type, synchronous carriers of multiple phase shifts with zero-crossing synchronization and Voltage reference of each carrier are required. This type is preferred to distribute power evenly among all the MLI modulus and hence support reduction in harmonic distortion. In the latter type only single carrier is sufficient to design and implement various levels of voltage. LS-PWM technique is further grouped into Phase Disposition PWM (PD-PWM), Phase Opposition and Disposition PWM (PODPWM), and Alternative Phase Opposition and Disposition PWM (APOD-PWM). The above-mentioned techniques comprise unipolar and bipolar carrier sections to enhance the fundamental output voltage and encourage total harmonic distortion reduction

II. RELATED WORK

Radhakrishna Das, et.al [2] proposed a method where the single phase inverters are modeled as a frequency changer and simulated it with a modulated Pulse Width Modulation (PWM). Pulse Width Modulation is employed to minimize THD in an inverter.

MATLAB - Simulink was utilized to implement the model integrated with SimPower System Block Set. Computer Aided Simulations play a predominant part in designing, analyzing and evaluating the power electronic converters and controllers. MATLAB has been extensively used in analyzing PWM inverter. MATLAB offers merits such as: Swift response, provide resource of various functional blocks and their simulation tools, free from convergence problems etc. Solving switching transients can offer Safe-commutation strategy.

Hence Insulated Gate Bipolar Transistor (IGBT) was preferred as a switching device. Moreover IGBT could be easily controlled to provide minimal loss.

MATLAB simulation was verified to provide better results prior to experimental verifications. A MLI based on double staged switched capacitor possessed the demerit of higher voltage stress in the second stage as reported in Sze Sing Lee [3]. In order to overcome this afore said issue, a switched-capacitor module (S3CM) with single stage for cascaded MLI was proposed that ensured the same Peak Inverse Voltage (PIV) across the switches within a DC voltage source.

A single DC source sufficed to generate 9 voltage levels embedding 2 incorporated capacitors. Therefore, a significant reduction in total number of isolated DC sources was reported in comparison with cascaded H-bridge. Besides, the method attained gain in voltage boosting. Comparative analysis was performed against the recent topologies that revealed the efficiency of the S3CM topology method in achieving reduction in switches.

Ehsan Najafi, et.al [4] proposed a multilevel inverter which is prominently accepted, suiting high-power and high- voltage requirements. The methodology provided better performance and outperformed the traditional two-level inverters as it resulted in minimized harmonic distortion, lesser Electromagnetic Interference (EMI) and established larger DC link voltages. At the same time, increase in number of used components, more complex PWM control method, and issues in voltage balancing were reported as some of its demerits. A novel topology involving reversed voltage component was presented to enhance the multilevel performance by the way of compensating the issues afore mentioned. This enhanced topology employed lesser components on comparing with existing such type inverters (higher levels). Few carrier signals, minimum gate drivers were also some of the specifications of the new method. This resulted in lower overall cost and reduced complexity for high levels of output voltage. A seven-level prototype topology was constructed and evaluated. A better performance of the inverter was attained by witnessing experimental results.

A Cascaded MLI was proposed by Marius Malinowski, et.al [5].

The method synthesized a low to medium output voltage depending on a power cells which are cascaded. The power cells utilize standardized low-voltage component configurations. This type of characteristic permitted high-quality voltage outputs and input currents. This method had a merit of outstanding intrinsic redundancy in component usage. Owing to these characteristic features, the cascaded MLI was recognized as a vital alternative in the area of medium-voltage inverter sectors. A categorical survey of various topologies, modulating techniques and control measure strategies were presented along with regenerative and advanced topologies.

Finally, future developments were addressed. Bouhali et al [6] reported a three-phase diode clamped inverter. Direct spaced line to line voltages were deployed as a control method embedded with voltage balance approach by a DC link capacitor. Anshuman Shukla et al [7] introduced certain control schema for equalization of DC capacitor voltages in diode clamped multilevel inverter.

An independent voltage control solar array was developed by Sergio et al [8] employed diode clamped converter at multiple levels for using in Photo-Voltaic (PV) generations. Partha P Biswas et al [9] developed a model in which unequal DC sources were considered with realistic supposition. Evolutionary algorithms were deployed to calculate the optimal DC voltages and switching angles so as to reduce THD. LSHADE-EpSin, a differential evolution was applied for optimization.

Lower order harmonics were eliminated using natural selection-based optimization approach in [11] proposed by Madhuri Mali and Patil. In [10] the authors made a comparison between different PWM techniques: Multi-Carrier, Sinusoidal and Selective

Harmonic Elimination for reducing THD in Cascaded H-Bridge MLI.Alternate Position of Disposition scheme was employed for switching pulse generation in MLIs. Optimization algorithms such as Genetic Algorithm (GA), Particle Swarm Optimization (PSO) algorithm were used in the latter method in defining the needed switching angles in reducing low order harmonics. Selective Harmonic Elimination Pulse Width Modulation method proved better in obtaining an optimal solution for reducing THD. Teena Jacob and Padma Suresh in [12] presented a review on bio-inspired algorithm based THD reduction in MLI. SHEPWM technique was proved to do better in reducing THD.

III. ANALYSIS OF MULTILEVEL INVERTER TECHNIQUES

3.1 Cascade H-Bridge Inverters

Cascading of H-bridges is performed in each phase. Hence total output voltage of the cascaded MLI is then the sum of individual bridge's output voltage. A staircase waveform could be generated in a controlled fashion.

The output tends to be more oriented towards sine waveform if more number of such H-bridges is connected in phase. A separate DC source is needed for the DC bus of each H- Bridge individually. Hence, this type of topology is utilized to collect energy from renewable energy resources such as fuel cells, solar cells etc.

3.1.1 Approched Circuits

To analyze the harmonics of different topologies, simulations of some PWM techniques were analyzed.

- Three level inverter
- Five level inverter
- Phase disposition
- Phase opposition disposition
- Alternate phase opposition disposition
- Phase shifted PWM

In the simulation of the various types of MLI's using different PWM techniques, we analyzed the harmonics through the FFT analysis tool in the MATLAB

3.1.2 Three Level Inverter

A three-level inverter is the basic of all multi-level inverters. The circuit is given in fig 1. There are basic four modes of operation.

Mode 1: Switches s1 and s2 of the three level cascaded H-Bridge inverter are switched ON. No source is connected to load. This results in no output voltage across the load.

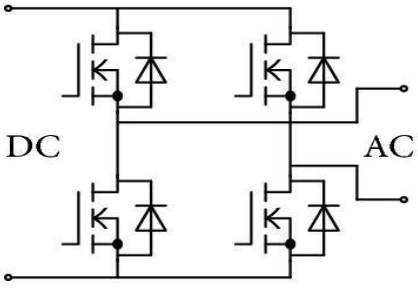

Fig 1 Circuit of Three Level Inverter

Mode 2: Switches s1 and s4 are turned ON. +V dc is obtained across the load.

Mode 3: Switches s2 and s3 are turned ON. –V dc is obtained across the load.

Mode 4: Switches s3 and s4 are turned ON. Zero Output voltage is obtained across the load.

Table 1 shows the operation.

Table 1: Switching pattern of 3 level inverter

Switches	+Vdc	0	-Vdc
S1	ON	OFF	OFF
S2	OFF	ON	ON
S3	OFF	OFF	ON
S4	ON	ON	OFF

A three level inverter with 230V input DC voltage and 50ohm is shown in Fig 2. At the output waveform we get an approximately 230v.

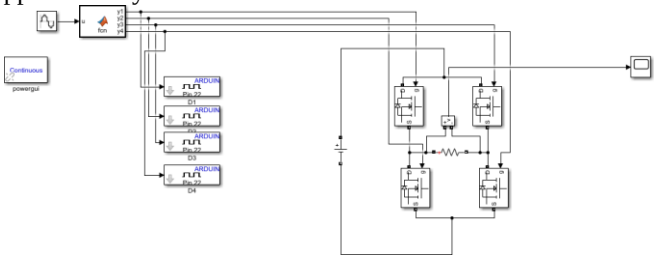

Fig 2 Simulation of 3 Level inverter

Fig 3 shows the simulated output of a three level inverter and Fig 4 shows the THD level

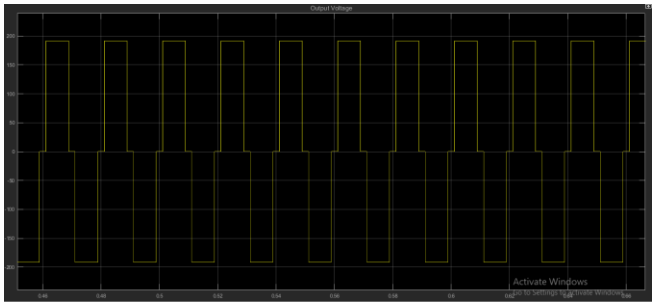

Fig 3 Output of a three level inverter

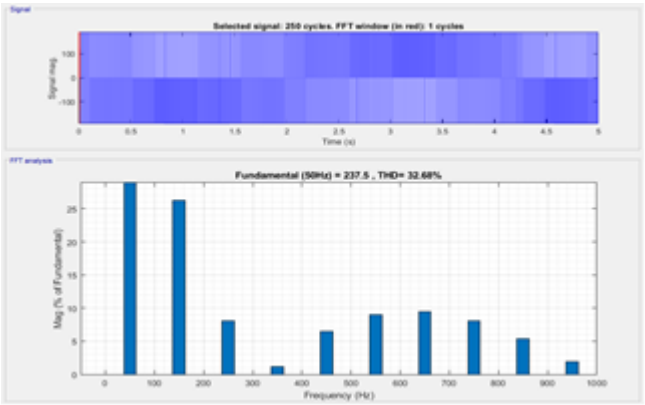

Fig 4 FFT Analysis of three level inverter with THD

3.1.1.2five Level Inverter

In five level inverter, the input DC voltage is given as 9 V in both the DC sources and the value of resistor is 50ohm. 18V output is obtained. A five level inverter is depicted in fig 5.

Simulated output is illustrated in fig 6 followed by THD analysis in fig 7

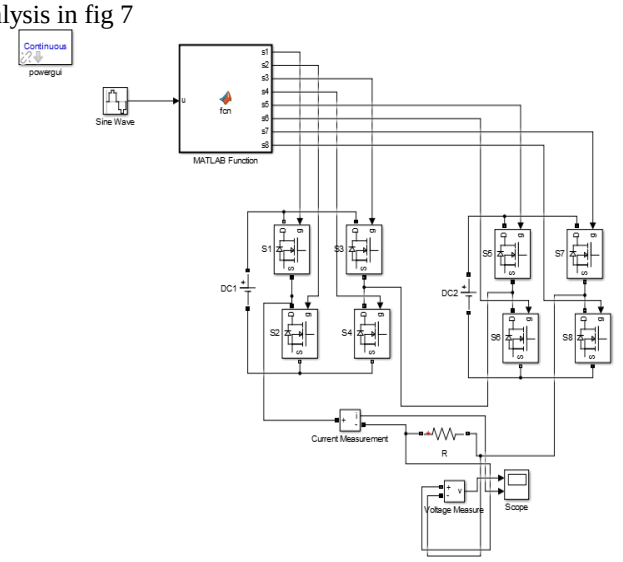

Fig 5 Five level inverter

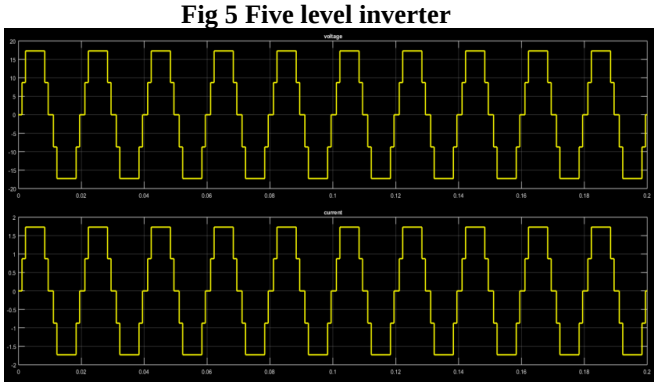

Fig 6 Simulated output of a five level inverter

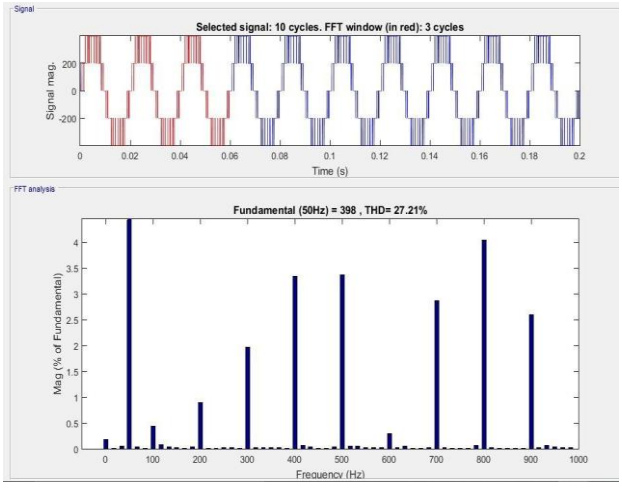

Fig 7 FFT Analysis of Five level inverter

Phase Disposition

In phase disposition (PD) modulation, all the carrier waveforms below and above the zero reference are considered in phase. Fig 8 represents the switching pattern of PD method.

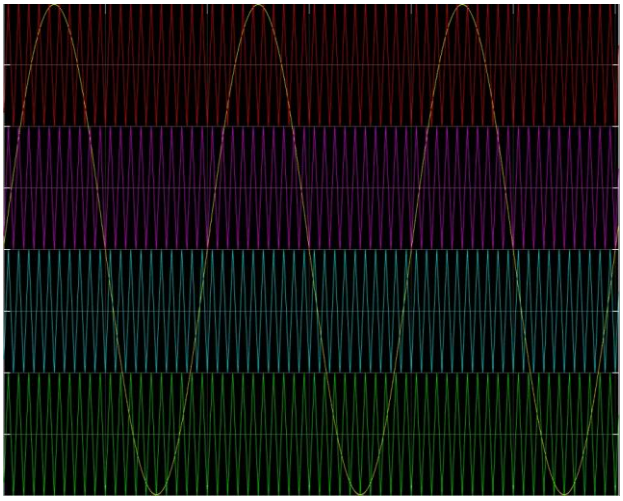

Fig 8 switching pattern of PD method

Rules followed for the phase disposition method with N = 5 are slated below.

- N –1 = 4 carrier waves are well arranged such that all the carrier waves below and above zero reference are available in phase. Two such carriers are below the zero line reference and the other two above the zero line reference.
- Once the reference goes higher than the first positive carrier waveform, the converter tries to switch to + Vdc and switches to the next level +2Vdc, if the reference goes higher than the second positive carrier waveform.
- If the reference goes lower than all of the positive carrier waveforms, a zero level is switched. It is applicable for negative carrier waveforms also.
- -Vdc is attained once the reference goes less than the first negative carrier waveform.

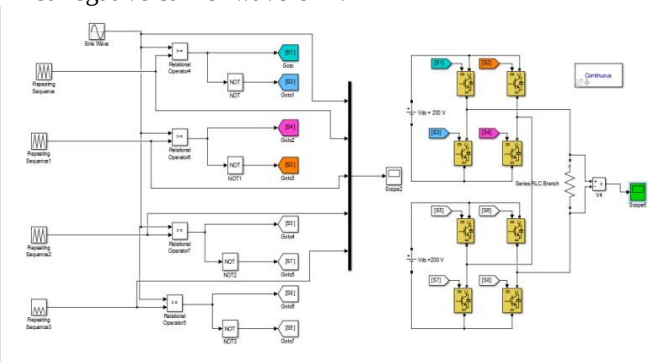

Fig 9 PD method

In this phase disposition inverter, the input DC voltage is given as 200v in both the DC sources and the value of resistor is 100ohm. At the output waveform we get an approximately 400v as portrayed in fig 9.

The output waveform taken from the MATLAB Simulink is shown in fig 10. Fig 11 points the FFT analysis of the method showing the THD obtained.

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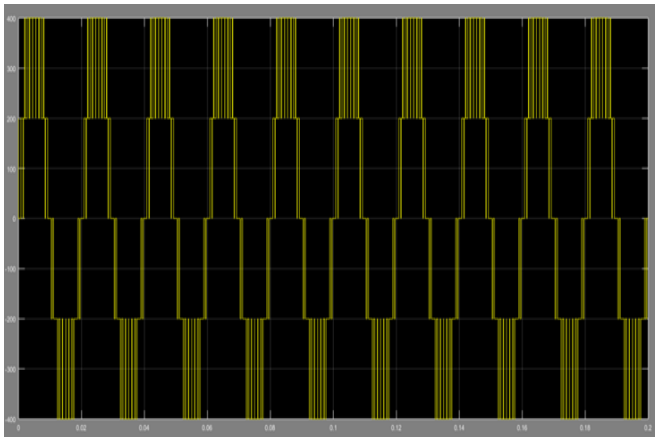

Fig 10 Output of PD method

Fig 11 shows the harmonics generated in the simulation of five level phase disposition inverter

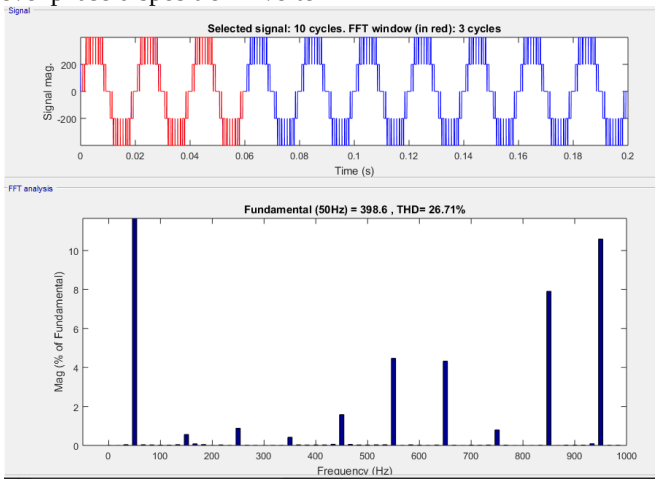

Fig 11 FFT analysis of PD method

3.1.1.4phase Opposition Disposition

For phase opposition disposition (POD) modulation all carrier waveforms above the reference zero are considered in phase and 180° out of phase otherwise. Switching pattern of POD is shown in figure 12

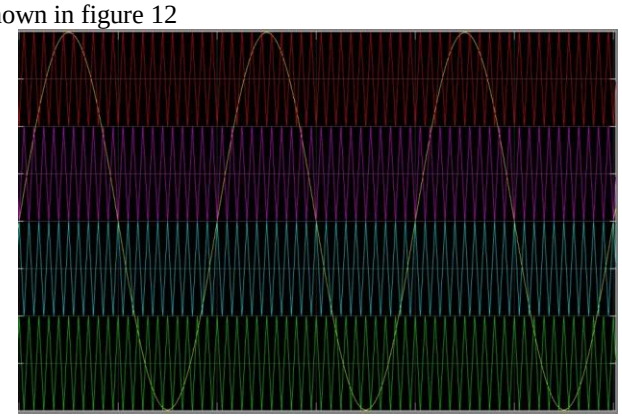

Fig 12 Switching Pattern of POD method

Keeping N = 5, the number of levels, certain rules framed in the phase opposition disposition method are

- N –1 = 4 carrier waveforms are so arranged that all the carrier waveforms higher than zero level are in-phase and 180 degree out of phase with those below zero. Two carrier waveforms are above the zero-reference line, while rest of the carrier waves with 180 degree shift are below the zero reference.
- +Vdc is switched by the converter as reference is higher than the first positive carrier while +2Vdc is switched once the reference goes higher than the second positive.

Negative similar is reached otherwise such as –Vdc and -2Vdc respectively

- Once the reference is lower than all the positive and negative carriers, the converter switches to zero.

In this Phase opposition disposition inverter the input DC voltage is given as 200v in both the DC sources and the value of resistor is 100ohm. At the output waveform we get an approximately 400v

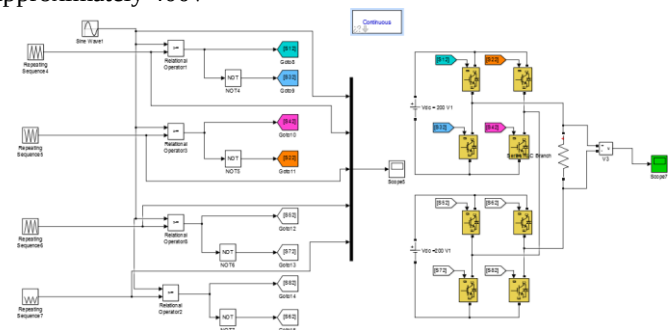

Fig 13 Schematic of POD Method

The output waveform taken through the MATLAB Simulink is illustrated in Fig 13 followed by FFT analysis (harmonics generated in the simulation of five level POD inverter) in fig 15

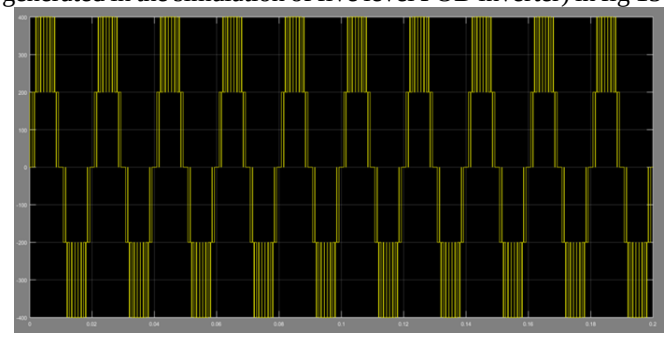

Fig 13 Simulink output of POD

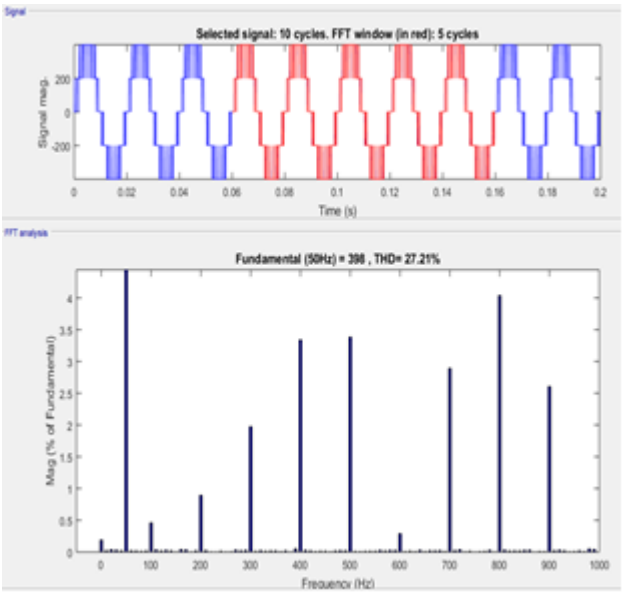

Fig 14 FFT analysis of POD method

3.1.1.5 Alternate Phase Opposition Disposition (Apod)

It is considered that each carrier is 180 degree out of phase with its neighbor. Fig 15 represents the switching pattern of APOD.

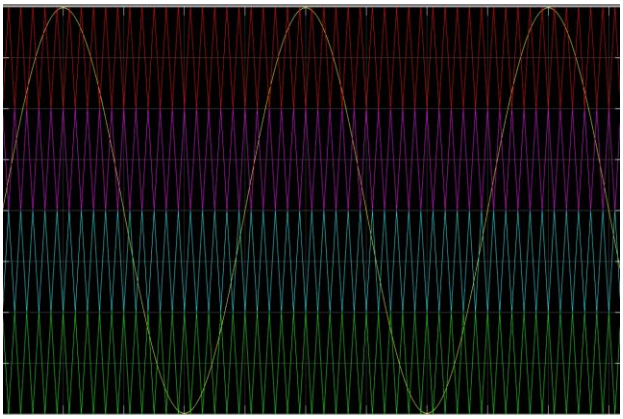

Fig 15 switching pattern of APOD

For N = 5, the rules governing APOD method are

- N – 1 = 4 carrier waveforms are so arranged such that each carrier signal is out of phase with its neighbor by 180 degree. Two positive carriers of positive magnitude and two negative carriers of negative magnitude are considered.
- + Vdc is switched once the reference goes past the first positive carrier and +2Vdc if the reference goes past the second positive and vice versa under negative conditions as seen before.
- Zero level is obtained if reference is lower than all the positive and negative carrier waveforms.

In this Alternate Phase opposition disposition method (APOD) inverter the input DC voltage is given as 200v in both the DC sources and the output waveform we get an approximately 400v. Fig 16 illustrates the APOD.

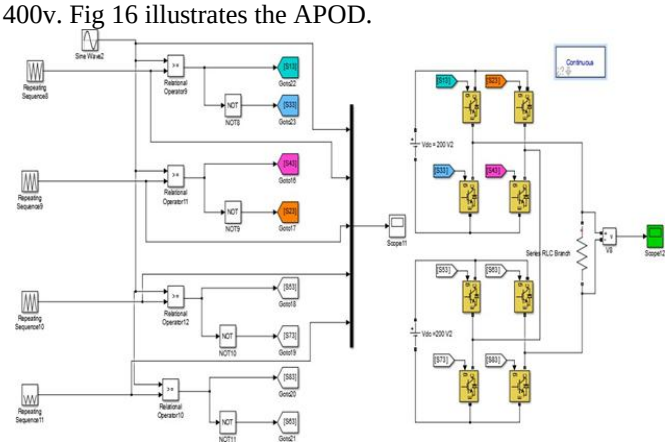

Fig 16 Schematic of APOD

The output waveform taken through the MATLAB Simulink is illustrated in Fig 17 followed by FFT analysis in fig 18.

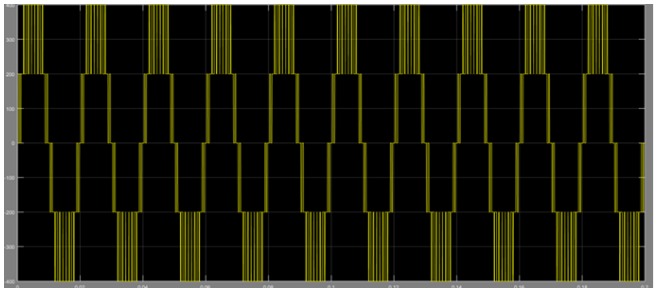

Fig 17 Harmonics generated from APOD

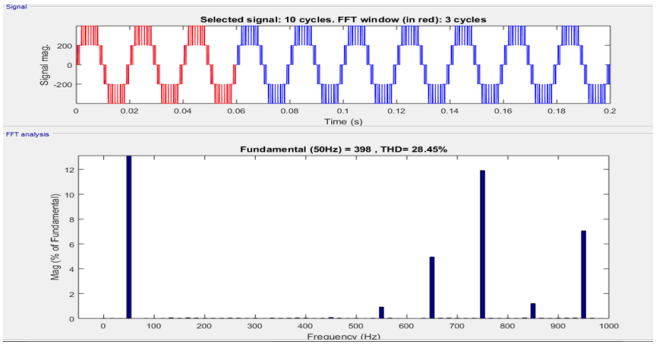

Fig 18 FFT analysis of APOD

3.1.1.6 Phase Shifted Pwm

In phase shifted PWM, similar Peak to Peak (P-P) amplitude and frequency is maintained in all triangular carriers. A phase shift is observed between any the adjacent carrier signals. For m defined voltage levels, the required carrier signals will be m-1. A phase shift of θ= (360°/m-1) exist between them. Gate signals are produced with proper modulating and carrier signal comparison. Fig 19 represents the switching pattern of phase shift PWM

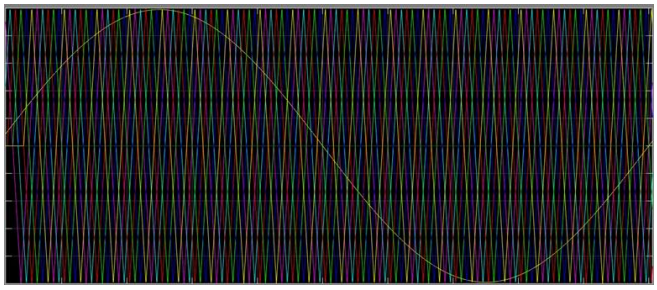

Fig 19 Switching pattern of phase shifted PWM

In this multi carries type inverter the input DC voltage is given as 200v in all DC sources and the value of resistor is 100ohm and 100mH inductance. At the output, 200V is obtained. Fig 20 shows the schematic followed by output from Simulink in fig 21 and FFT analysis showing THD in fig 22.

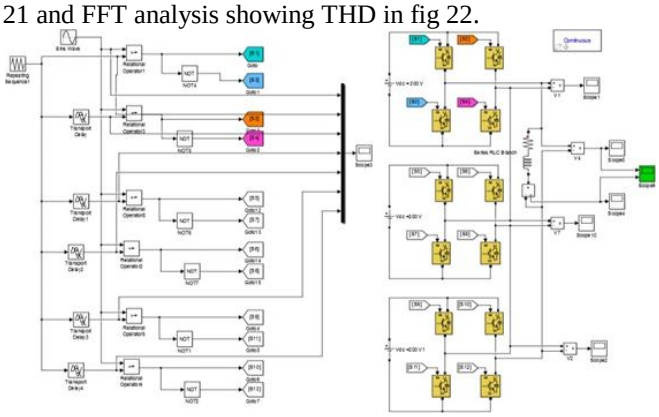

Fig 20 Phase Shifted PWM

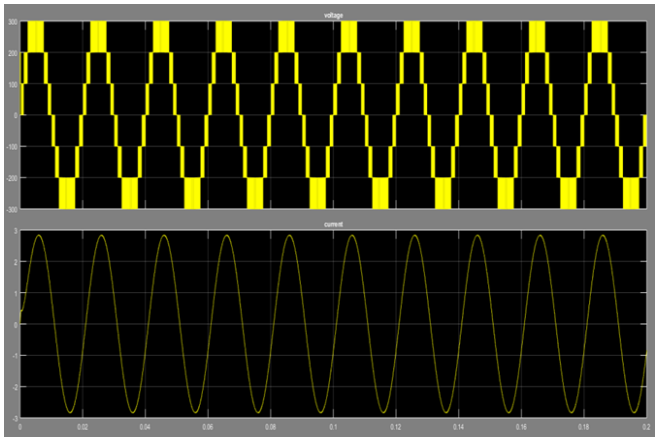

Fig 21 Simulink output of Phase Shifted PWM

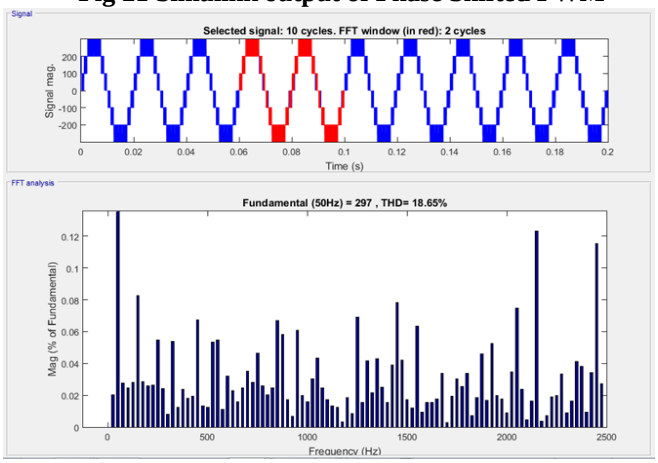

Fig 22 FFT analysis of phase shifted PWM

IV. HARMONIC ANALYSIS

4.1 Even Harmonics

Nonlinear loads generally generate ODD harmonics. Hence EVEN harmonics such as second, fourth and sixth rarely occur which are detrimental to any electrical system. If both positive and negative half cycles are similar and are subjected to Fourier series, the resulting series will have only ODD harmonics.

4.2 Odd Harmonics

ODD harmonics such as third, fifth and seventh are most common forms in electrical power system leading to multiple consequences if left uncontrolled. Any of the sequential component either positive, negative or even zero will be in relation with each and every odd harmonic. Phase sequence is really vital as it estimates the adverse effect of such harmonics on the functioning of electrical power equipment. Table 2 illustrates the harmonics and the phase sequence associated with it.

4.3 Causes Of Harmonics

Harmonics are generated by loads having non-linear properties which draw a non- sinusoidal current from a voltage source of sinusoidal type. Some of the non-linear loads include Static VAR compensators, inverters, Electric Arc furnaces, Motor drives, SMPS, DC converters.

Table 2 Comparison of Different types of MLIs with the THD obtained

Types	Total harmonic distortion%
3 level cascaded	32.61
5 level cascaded	27.21
Phase disposition	26.71
Phase opposition disposition	27.21
Alternate Phase opposition disposition	28.45
Phase shifted	18.65

The table shows the harmonics of analyzed techniques. It is clear that the harmonic level in the phase shifted method is better when compared with other techniques.

V. CONCLUSIONS

A comparison of the different MLI technique in reducing the THD is carried out based on different Pulse Width Modulation. The high frequency pulse width modulation methods are analyzed with the simulation results. The Simulink model for inverter has been implemented through MATLAB. The resulting current and voltage graphs are studied. From the above discussion, the multi-level inverter with a phase shifted pulse width modulation gives comparatively less total harmonic distortion of 18.65%. It can be concluded that high frequency techniques have the ability to reduce the total harmonic distortions.

CONFLICT OF INTEREST

Authors declare no conflict of interest and funding

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