Design and Implementation of Rearrangable Non-Blocking Switching Network in VLSI

B. Swapna Rani , C.Chitra

Abstract— The main goal of this article is to implement an effective Non-Blocking Benes switching Network. Benes Switching Network is designed with the uncomplicated switch modules & it's have so many advantages, small latency, less traffic and it's required number of switch modules. Clos and Benes networks are play a key role in the class of multistage interconnection network because of their extensibility and mortality. Benes network provides a low latency when compare with the other networks. 8x8 Benes non blocking switching network is designed and synthesized with the using of Xilinx tool 12.1.

Keywords: Benes Network, Non-Blocking Switching Network, Clos Network, Blocking Network, Cross Bar Switch.

I. INTRODUCTION

All of us actually use telephones and all of us use to browse through internet and we all our check emails through every day through on browser and we do may setup TCP connections but these all are worked based on communication. In case of telephony we have exchanges in case of internet we have routers and data will be routed finally it will reach the destination source and the flow of the information happens in the both directions.

Switching is the important asset to the networking. The exchanging of information or data between the network segments or different networks is called as a switching network. In switched network, data or information entering to the network from a mainframe (computers, terminals, telephones or other communication networks) by switching the data from node to node the data is routed to the destination source. Simple Switching Network is illustrated in below figure1.

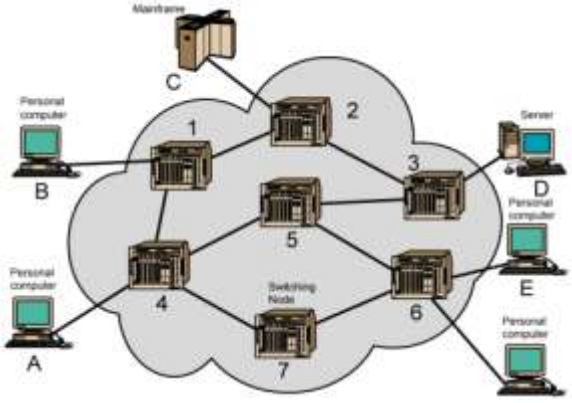

Figure1: Simple Sample switching network

Switched networks are derived into the different networks those are circuit switched networks; packet switched networks and messaged switched networks. Packet switched networks are derived into two types those are datagram networks and virtual circuit networks. Switching can increase the speed and capacity of your network. In the network, same like hubs switches also occupy the same place. To improve the speed of the network parallel algorithms are proposed. The need of parallel processing algorithm is an initiated to build faster system. High speed and faster interconnects are been gained the lot of attention from computer industry, interconnects is became a limited aspect to the achievement of present day computer systems. The messages routing is a key to achievement of that networks. Parallel algorithms are used to speed the routing in network. In Network, The interconnection plays a virtual role and it is the important key factor in parallel computer. The interconnection networks are divided into the two types those are direct and indirect networks. In direct network method each switch is directly linked with the actual processing node. Different topologies are proposed with the using of direct network method. In the Indirect network the each node is connected to a network switch over one or more bidirectional links.

The Multistage interconnection networks are indirectly connected to the processors via different layers of switches or intermediate nodes. The better parallel algorithm provides the best results like less time complexity (Execution time) and low space complexity (The amount of memory). In this article Non Blocking switching network is proposed. In below section we will discuss Blocking switching network and Non Blocking Switching Network.

II. BLOCKING SWITCHING NETWORK:

- In blocking switching network, inputs are not connected to the outputs nothing but there is no path between the inputs and outputs. The all possible intermediate switches are busy with the other sources so no path will be there between the input and output.
- In Blocking switching network, at a time read and data is not possible so it needs the time for the acknowledgement so automatically latency time will be increased.
- In Blocking Switching Network, Sending the data and receiving the data on same time will not possible.

The basic design of Blocking Switching network is illustrated in figure2.

Revised Version Manuscript Received on 10 September, 2019.

B. Swapna Rani , Associate Professor, TKRCET, Medbowli, SAROOR NAGAR, Hyderabad, Telangana, India.(Email: swapnaharshith@gmail.com)

Dr. C.Chitra, Professor, SSSUTMS, Sehore, Bhopal, M.P, India.

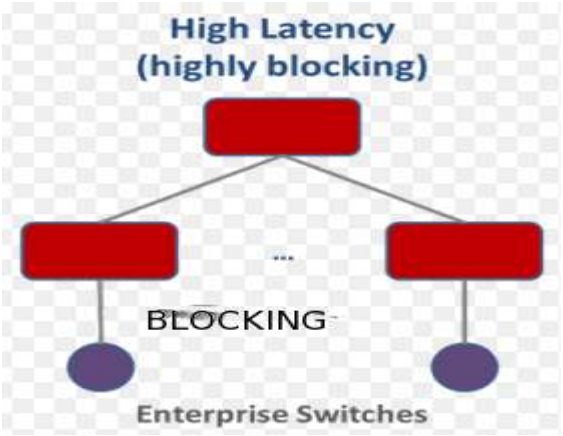

Figure2: Blocking Switching Network

III. NON-BLOCKING SWITCHING NETWORK:

- In non-blocking switching network, inputs are connected to the outputs nothing but there is path between the inputs and outputs.
- In non-Blocking switching network, at a time we can read the data and we can write the data so it needs the less time for the acknowledgement. The Application can respond to reading data from the source and which sends some data back to the source.
- Non blocking switching network performs the immediate operation for sending and receiving data and it's not waiting for the any acknowledgment.

The sample design of non blocking switches is shown in below figure3.

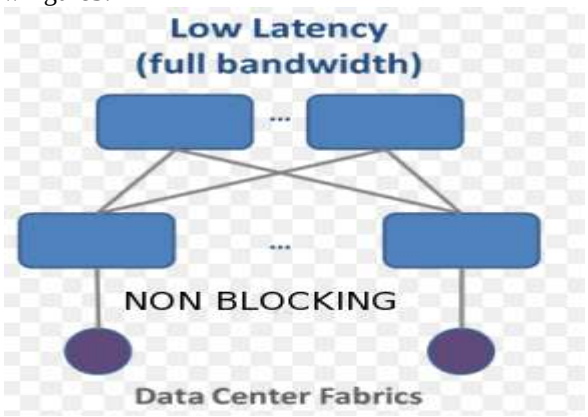

Figure3: Non Blocking Switching Network.

The non blocking switching network is designed with the cross bar switches. Cross bar switches are discussed in below section. Non blocking switches are providing the low latency. Like cross bar switches the non blocking switches also provides the full connectivity in the network.

IV. CROSS BAR SWITCH:

Cross bar switch is a switch which connects the multiple inputs to the multiple outputs in a manner of matrix and it's also called as a matrix switch and cross-point switch. Actually, the crossbar switch exposed the crossing metal bars and which provides the paths for input and output. Let's considered that the cross bar switch have the M inputs and N outputs then the crossbar switch provides the matrix with the form of MxN. At the each cross point of switch is closed its creates a connection for one of the input to the one of the output. Cross bar switches are used in the Benes network.

Cross bar switches are used in so many applications those are circuit switching and telephony. Crossbars switches are the widely used components of rising multistage interconnection networks among all components and in the different networks like local area network, metropolitan area network and wide area network. The sample design of Cross bar switch is shown in below figure4.

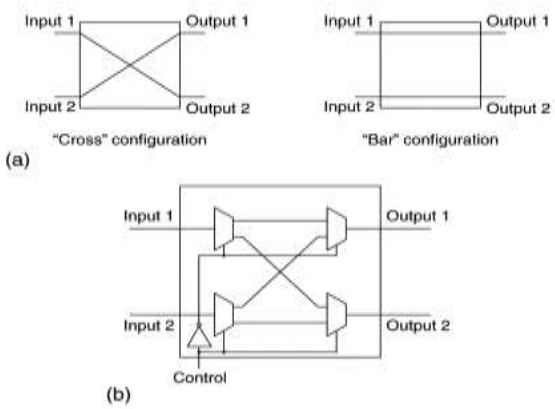

Figure4: Cross bar switch

Benes Network:

In 1962, scientist BENES proposed the one permutation network with his name that is the Benes Network. N input and N output benes network is derived by the B(N). The benes network is the rearrangable non blocking network. This benes networks are used in the parallel algorithms and computer networks. The benes network also used in the SIMD (Single instruction stream and multiple data stream) to compute the interconnections to the N processing elements. The structure of Benes design is showing in below figure5.

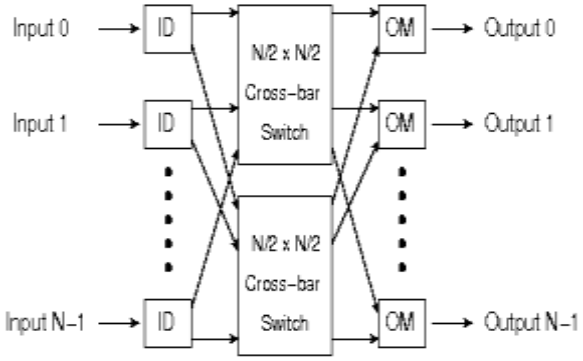

Figure5: Structure of Benes Network B(N)

A Benes network is simply a butterfly network with the N inputs and N outputs. Those networks have the $2\log_2 N - 1$ stages. It's contains $N/2$ 2×2 crossbar switches, which use a total of $N\log_2 N - N/2$ 2×2 crossbar switches. The input and output mappings implemented by the 2 x 2 crossbar switches and it's includes the upper and lower broadcast mappings ui(x) and li(x),

Where ui(x) = an, ... , ai+1, 0, ai-1, ... , a1 (upper broadcast Mapping)

And li(x) = an, ... , ai+1, 1, ai-1, ... , a1 (Lower broadcast Mapping)

The upper broadcast mapping and lower broadcast

mappings are shown in below figure6.

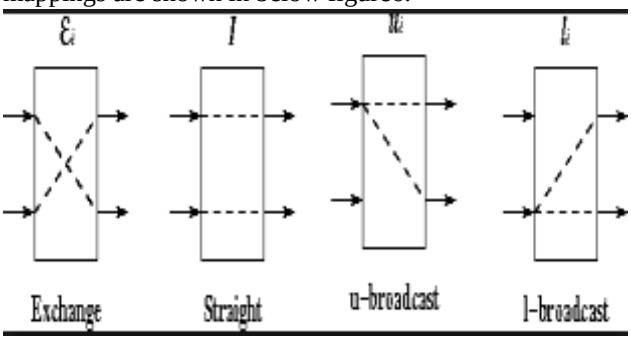

Figure6: Broadcast Mappings

For example, am taking a 8x8 Benes network nothing but 8 number of inputs and 8 number of outputs. It has $2\log_2 8 - 1 = 5$ stages and N/2 2x2 crossbar switches here N=8, so it's have 4 2x2 cross bar switches. The design of 8x8 Benes network is shown in below figure7. Simply, the 8x8 Benes switching network have the 5 stages and 4 2x2 crossbar switches.

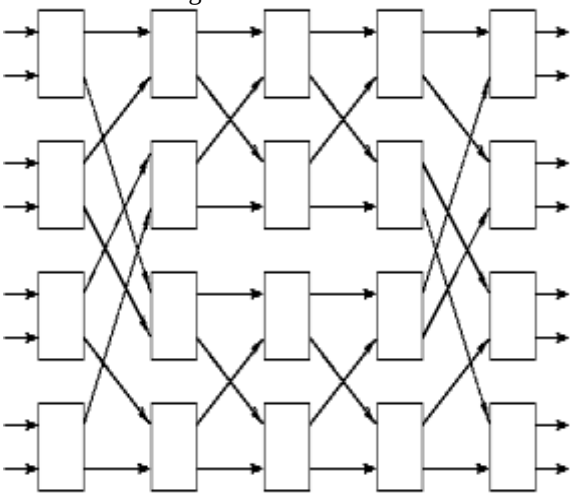

Figure7: 8x8 Benes Network

Large size Benes networks are designed with the smaller Benes networks. The 8x8 Benes network is designed with the help of 2x2 Benes networks. In Benes Network, number of inputs and outputs are increased then automatically number of stages is increased. In figure7, the center part three stages has 2 4*4 Benes network. The 4*4 Benes network, can connect the any input to the any output respectively.

V. SIMULATION RESULTS:

The Non-blocking switching network (Benes Network) provides the low latency and which not waits for any ACK to send data and receive data. Here we are designing the 8x8 non blocking switching Networks with the use of cross bar switches. We know that Benes network is rearrangable switching network. The Synthesis and simulations are done by Xilinx 12.1 and the output results are accurate according to the design. The Simulation Results are shown in below figures.

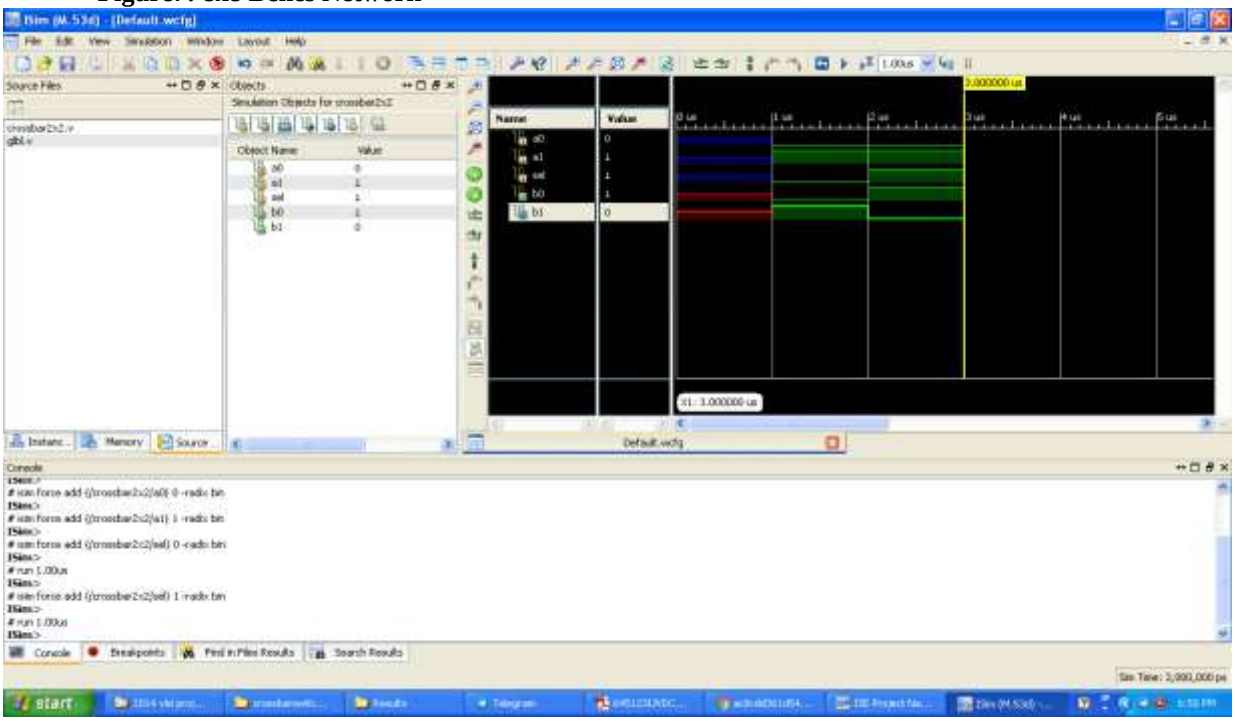

Figure8: Simulation Result of 2x2 Benes Network

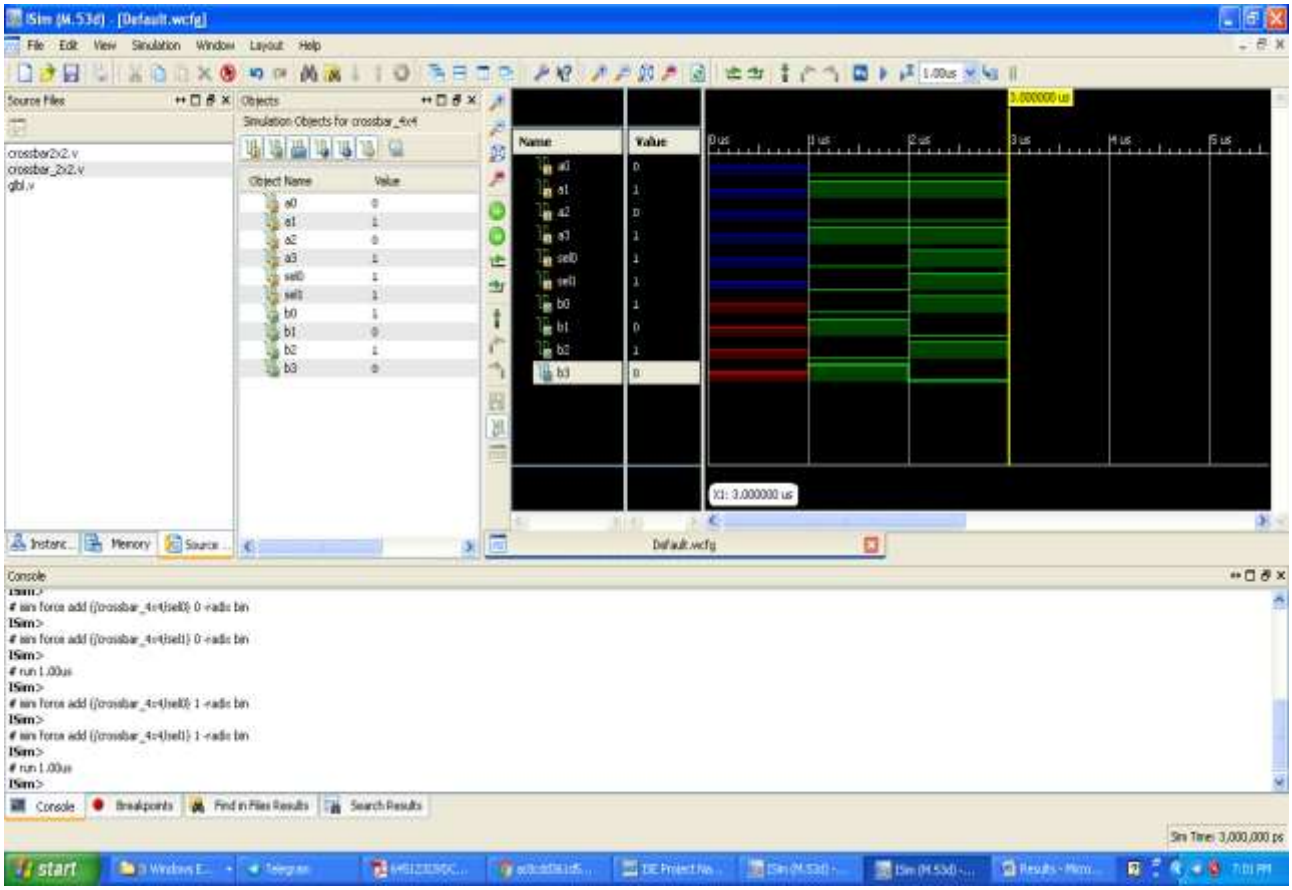

Figure9: Simulation Result of 4x4 Benes Network

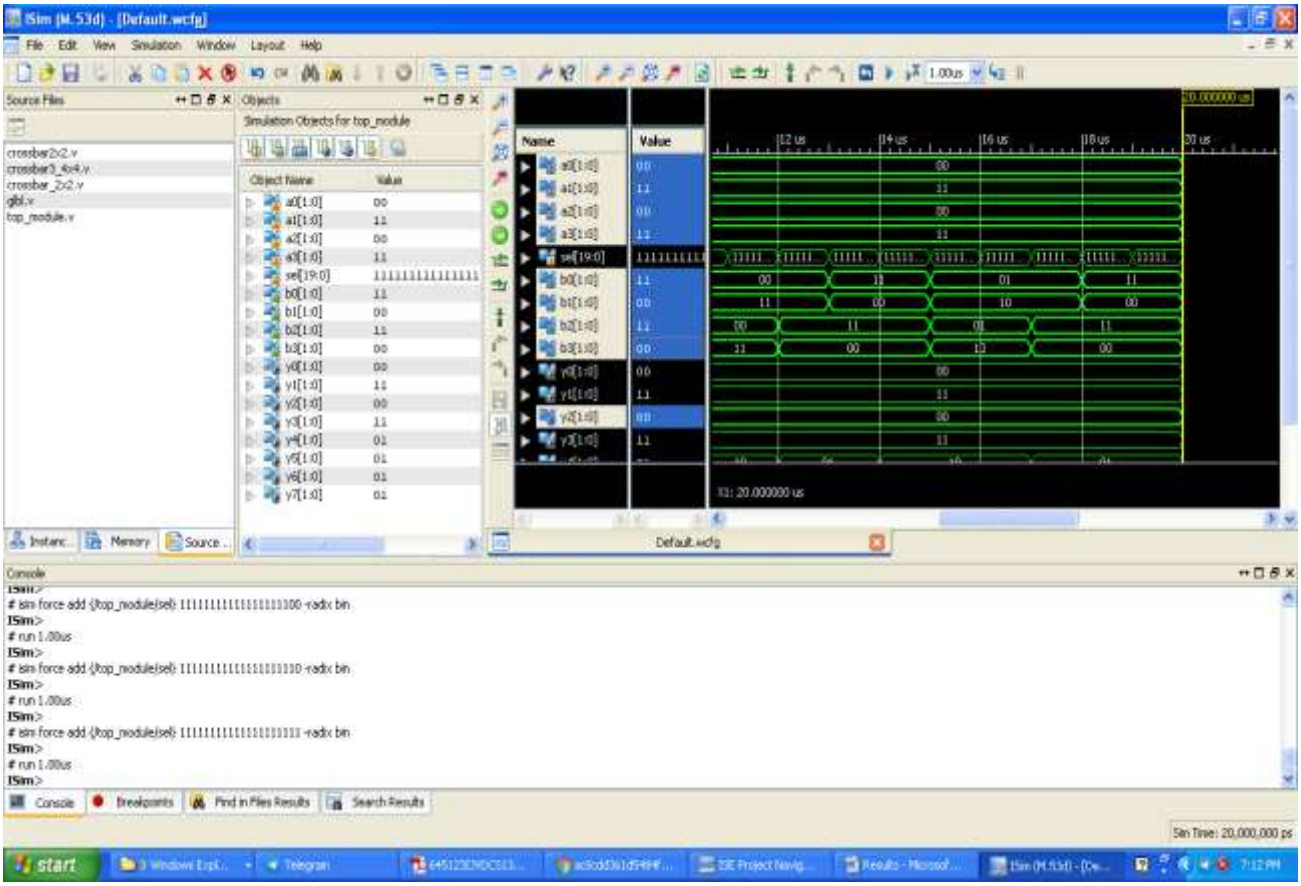

Figure 10: Simulation result of 8x8 Benes Netork

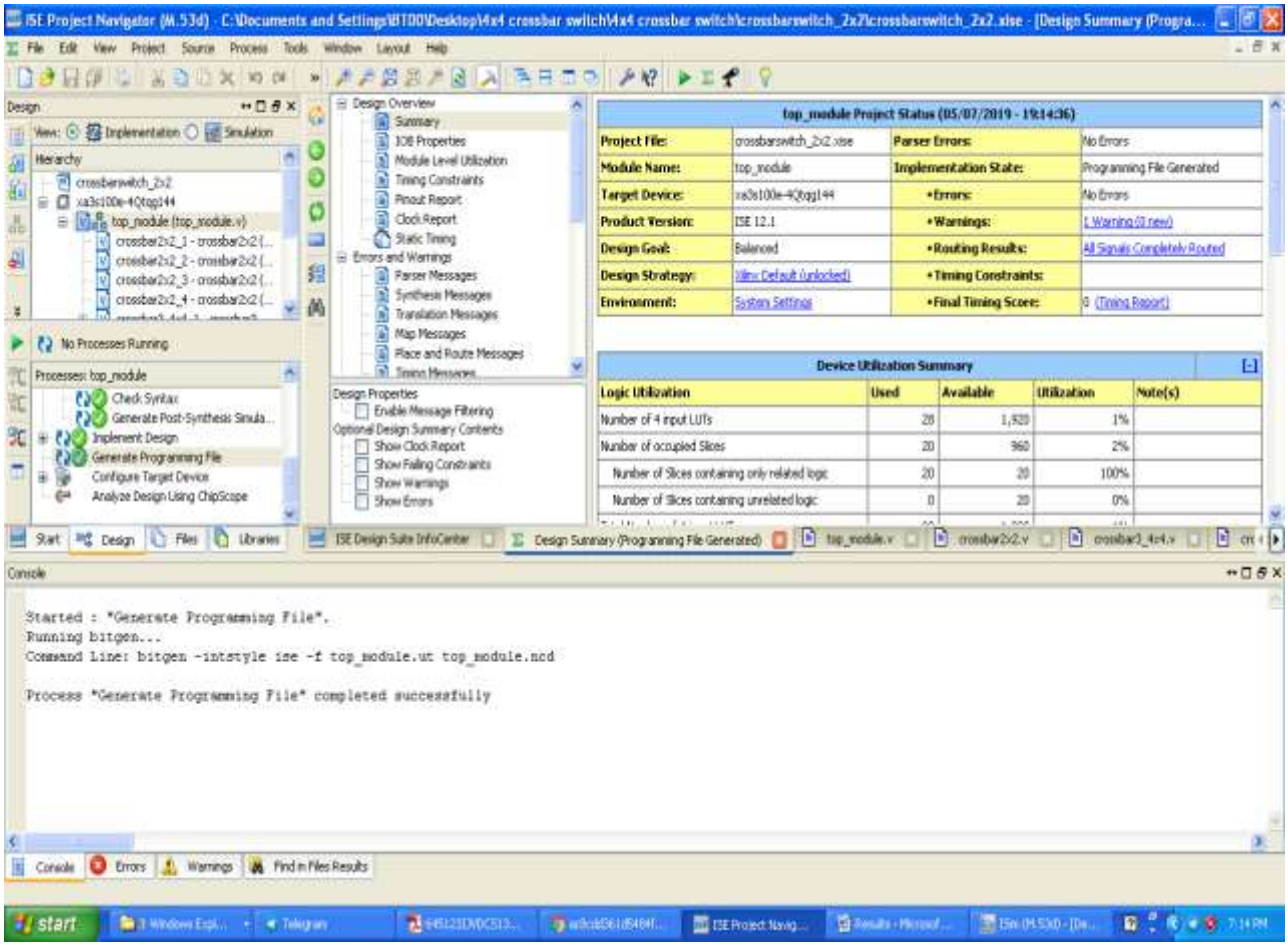

Figure11: Design Summary Of 8x8 Benes Network The

Design Summary provides the information about the 8x8 Benes Network has taken how many Lookup tables and how many slices are used in the design, delay and Memory. Here The 8x8 Benes Network design occupied the 20 slices its uses the 28 Look up tables and the delay is 8.218ns.

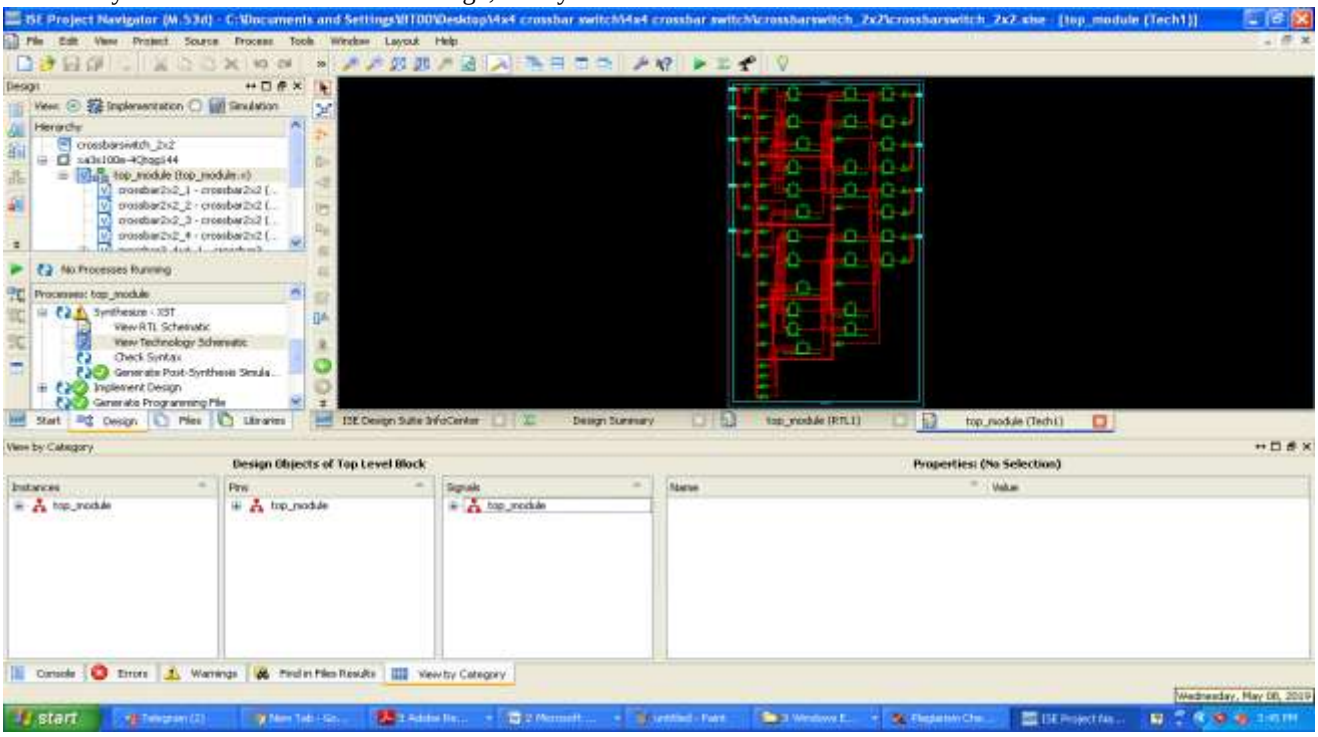

Figure9: RTL Design of 8x8 Benes Network

VI. CONCLUSION:

In this article, we presented a 8x8 Benes Network (Rearrangable Switching Network) which provides the low latency when compare with the Blocking switching network. The RTL Design of 8x8 Non blocking switching network has been fully implemented by the Verilog HDL. Benes Network is simulated and synthesized by Xilinx 12.1 tool. This article provides a further investigation on Non Blocking switching Network for other topologies. In the future, we can implement the 16x16 and 32x32 Benes networks with the use of 8x8 Benes Network.

REFERENCES

1. Abhay B. Rathod, S. M. Gulhane, A. R. M. Khan, “Parallel Routing Algorithms in Benes and Clos Networks”, Volume 2, Issue 1.
2. Yikun Jiang, “ Design and implementation of Benes/clos on chip interconnection Networks”(2016).
3. Longbo Huang, Jean Walrand, “A Benes Packet Network”, EECS department of University of California
4. Dimitrios Serpanos, Tilman Wolf, in Architecture of Network Systems, Interconnects and switching fabrics”, 2011.
5. Abbas karimi, kiarash aghakhani, “A Novel Routing Algorithm in Benes Network”, vol no.7 2016.
6. T.T. Lee , Soung-Yue Liew, “Parallel routing algorithms in Benes-Clos networks”, IEEE, 06 August 2002
7. Riccardo melen, Jonathan S. Turner , “Non Blocking Networks for fast packet switching”, IEEE, 1989
8. Yikun Jiang; Mei Yang. “Hardware design of parallel switch setting algorithm for Benes networks”, Vol 7, 2017.
9. BARRY G. DOUGLASS, A. YAVUZ ORU¸C, “ON SELF-ROUTING IN CLOS CONNECTION NETWORKS”, Institute of Advanced Computer Studies University of Maryland College Park.
10. SANJEEV ARORA , F. THOMSON LEIGHTON , AND BRUCE M. MAGGS, “ON-LINE ALGORITHMS FOR PATH SELECTION IN A NONBLOCKING NETWORK”, AMS