

Design of Variable Fractional Delay Filter using FIR Filter Approximation

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Abstract: Beamforming plays an important role in the field of wireless communication. Beamforming means combination of a radio frequency (RF) signals from multiple antennas to form a single direction beam. This technique improves the quality of communication and reduces the interference of signal. In beam forming technique, different phases signals can be achieved with different signals and the received phase delay signals are converted into same phase, multiply with weight factor and combined this signals to form a beam in desired direction. The required phase delays are generated by using a Variable fractional delay filter. Variable fractional delay filter is design by using a direct form of a FIR filter structure. Variable fractional delay filter is calculated by two different phase signals from digital antennas and those two different phase signals are converted to in-phase and added together to form a beam forming. As the order of the filter increases, the delay also increases. The filter coefficients of the variable fractional delay filter are calculated my using a Lagrange interpolation method. The variable fractional delay filter is designed by using software Xilinx version 14.3.

Keywords: Beamforming, Lagrange interpolation method, Phase delay, Variable fractional delay.

I. INTRODUCTION

Now a days in Digital Signal Processing applications, a fractional delay (FD) of a signal is used to replace a unit delay. Fractional delay includes echo cancellation, modeling human voice pitch, musical signal analysis, sampling rate conversion, and timing synchronization. For most of these applications, a real-time adjustable fractional delay value must be updated. A variable fractional delay (VFD) filter is required for all these applications that take a sampled signal input and re-sampled fractionally delayed signal as an output [1,2]. The main purpose of this work is to create a new filter that can delay a signal with an arbitrary sized delay between sample points. The previously explored implementations of this application have been able to delay signals with no variable and variable fractional delays in DSP processor [3].

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The main premise for this application is to interpolate the values between sample points to achieve a recreated delayed signal. Using this very rudimentary example, it is visually evident of the desired delayed signal at each of the sampling points.

The design of VFD filters is based upon manipulating available sampled data to interpolate the desired delayed signal by reducing the error of the approximated and actual delayed signal. Since the 18th century, the system designs and the mathematical calculations and algorithms such as Lagrange interpolation [4, 5] has came into existence. These algorithms and the implementations have been presented in several papers across all over engineering community. The Farrow structure, the maximally flat Lagrange interpolator, and other IIR VFD filters have been extracted from a theoretical design point. DSP processors are often used to implement these filters. Sampling rate, output flow rate, and bandwidth, DSP hardware bottlenecks, bus performance and a limited number of computational units are the limitations for these DSP processors.

Beamforming is the main application of fractional delay filter. The signals interfere with each other when they share the same frequencies, the same propagation direction, and the same polarization, which shows the property of beamforming. Generally, Signals can be canceling out with destructive interference and sometimes can be added up with constructive interference. Either by transmission or reception of signals spatial filtering devices can be created by beamformers in a specific direction.

The word "beamformer" suggests that beams are created and that beamforming aims its transmission only at one target. However, this is not always the case as selective reception can also be called beamforming.

II. BEAMFORMING TECHNIQUES

To create a pattern of constructive and destructive interference in the wavefront and to change the directionality of the array, a beamformer controls the phase and relative amplitude of the signal at each transmitter. Information from different sensors are combined in a way to get the preferable expected pattern of radiation at the receiver. "Phase shift" is the time delay unit in Narrow band systems, the array of antennas, and each one is shifted a slightly in different amount, which is called a phased array. In radars, narrow band system is the one where the bandwidth is of small fraction of the center frequency, where as in wide band systems these fractions do not hold longer, which is typical in sonar.

In the beamformer receiver, the signal from each antenna is amplified by a different weight. To achieve the desired sensitivity patterns, different weight patterns are used. A main lobe is produced together with nulls and the side lobes.



Design of Variable Fractional Delay Filter using FIR Filter Approximation

The position of a null can be controlled by controlling the width of the main lobe and the side lobe levels. By using this, the noise can be reduced while listening for events in other directions. A similar result can be obtained on transmission.

Beamforming techniques can be divided into two categories:

- Conventional (fixed or switched beam) beamformers
- · Adaptive beamformers or phased array
 - 1) Desired signal maximization mode
 - 2) Interference signal minimization or cancellation mode

First, the Conventional beamformers use a fixed set of weightings and time-delays to combine the signals from the sensors in the array, by using the information about the location of the sensors in space and the wave directions of interest. Secondly, the adaptive beamforming techniques generally combine this information with properties of the signals received by the array, to reduce the unwanted signals from other directions. This process may be carried out either by time or the frequency domain.

The name itself says that, an adaptive beamformer is able to automatically adapt its response to different situations. Some criterion has to be set up to minimize the total noise output frequency, in wide band systems it may be desirable to carry out the process in the frequency domain.

III. DESIGN OF VARIABLE FRACTIONAL DELAY FILTER

Variable fractional delay has the characteristic of updating the value of delay time online during the processing of input signal. There are two main design approaches using FIR approximations such as time domain and frequency domain approaches which includes sinc windowing, spline function, weighted least squares, Oetken's method, Lagrange interpolation and Farrow structure [6-10]. These design approaches are implemented and the magnitude and phase delay response are analyzed. Lagrange interpolation is observed to be the most attractive method from the time domain approaches since it has a smooth magnitude response. Farrow structure is preferable in the frequency domain approaches as the main advantage is that the filter coefficients are fixed.

The proposed Farrow structure uses Lagrange interpolation that has an advantage of being a fixed coefficient filter for a given order and real time control of delay. The design of proposed Farrow structure is made using inverse Vander monde matrix, which results in less number of multiplications than the conventional Horner's structure. Further, the complexity of the proposed Farrow structure is reduced by using the transformation matrix that is called as modified Farrow structure.

(A) Lagrange Interpolation method:

Lagrange interpolation is usually implemented using a direct-form FIR filter structure. It has several advantages such as easy explicit formulas for the coefficients, very good response at low frequencies, and a smooth magnitude response.

An alternative structure is obtained approximating the continuous time function $X_{\rm c}(t)$ by a polynomial in D, which is the interpolation interval or fractional delay. The

interpellants, i.e., the new samples, are now represented by (1).

$$y(n) = x(n - D) = \sum_{k=0}^{N} c(k) * D^{k}$$
 (1)

That takes on the value x (n) when D=0. The coefficients c (k) is solved from a set of N+1 linear equations. Farrow has suggested that every filter coefficient of an FIR interpolating filter could be expressed as an Nth-order polynomial in the delay parameter D. Hence, this result in N+1 FIR filters with constant coefficients. The alternative implementation for Lagrange interpolation is obtained formulating the polynomial interpolation problem in the z-domain as in (2).

$$Y(z) = H(z) X(z)$$
 (2)

Where X (z) and Y (z) are the z-transforms of the input and output signal, x (n) and y (n), respectively, and the transfer function H (z) is now expressed as a polynomial in D given by (3).

$$H(z) = \sum_{k=0}^{N} c_k(z) * D^k$$
 (3)

The familiar requirement that the output sample should be one of the input samples for integer D may be written in the z-domain as following (4).

$$Y(Z) = Z^{-D}X(Z)$$
 for $D = 0, 1, 2, ..., N$ (4)

Together with (2) and (4), this leads to the following N+1 condition given by (5).

$$\sum_{k=0}^{N} C_k(Z) * D^k = z^{-D} \text{ for } D = 0,1,2,3.....N (5)$$

This can be expressed in matrix form as given by (6).

$$U*C=Z (6)$$

Where the N*N matrix U is given by (7).

$$\mathbf{U} = \begin{bmatrix} \mathbf{0}^{0} & \mathbf{0}^{1} & \mathbf{0}^{2} \\ \mathbf{1}^{0} & \mathbf{1}^{1} & \mathbf{1}^{2} & \dots & \mathbf{1}^{N} \\ \mathbf{2}^{0} & \mathbf{2}^{1} & \mathbf{2}^{2} & \dots & \mathbf{2}^{N} \\ \vdots & & \vdots & & \vdots \\ \mathbf{N}^{0} & \mathbf{N}^{1} & \mathbf{N}^{2} & \dots & \mathbf{N}^{N} \end{bmatrix} = \begin{bmatrix} \mathbf{1} & \mathbf{0} & \mathbf{0} & \mathbf{0} \\ \mathbf{1} & \mathbf{1} & \mathbf{1} & \dots & \dots & \mathbf{1} \\ \mathbf{1} & \mathbf{2} & \mathbf{4} & \dots & \dots & \mathbf{2}^{N} \\ \vdots & & \vdots & & \vdots \\ \mathbf{1} & \mathbf{N} & \mathbf{N}^{2} & \dots & \dots & \mathbf{N}^{N} \end{bmatrix}$$
 (7)

(B) Variable fractional delay filter based on farrow structure:

The block diagram of fractional delay filter based on Farrow structure is shown in Fig. 1. It consists of 6 groups 5-order FIR filters.





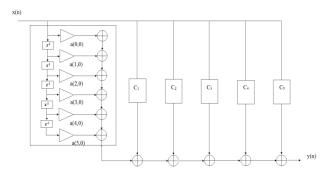


Fig. 1.Fifth order variable fractional delay filter block diagram

The 5th order variable fractional delay filter is shown in figure1.it consists of 6-group 5-order FIR filters. The filter coefficients are calculated by using a Lagrange interpolation method. Q (N, N) is the filter coefficient and N is order of the filter. Coefficients are calculated by using a Lagrange interpolation method. Q (N, N) is the filter coefficient and N is order of the filter.

IV. SIMULATION RESULTS

The Variable fractional delay filter using FIR filter is developed in Verilog HDL, Simulated using Xilinx ISE simulator and synthesized using Xilinx XST (Xilinx synthesis tool). The design code is simulated on the Xilinx

7k325tffg900-2. Input to a variable fractional delay filter signal is shown in Fig. 2 and considered as 19 digital inputs as shown in Table I.

Fig. 2 shows the analog signal input to a variable fractional delay filter. This analog signal is converted into digital signal and converted into IEEE 754 format. This IEEE 754 format sequence is taken as an input signal to a Verilog code of variable fractional delay filter.

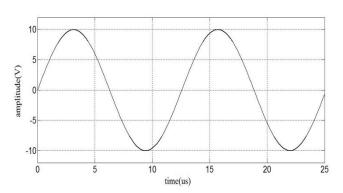


Fig. 2.Input to a variable fractional delay filter

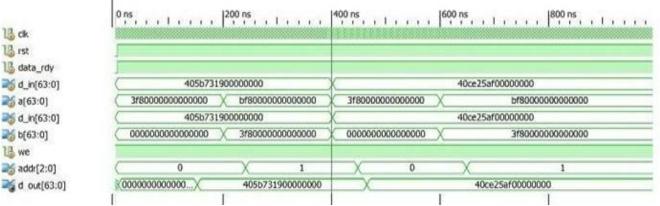


Fig. 3.Simulation results of first order variable fractional delay filter

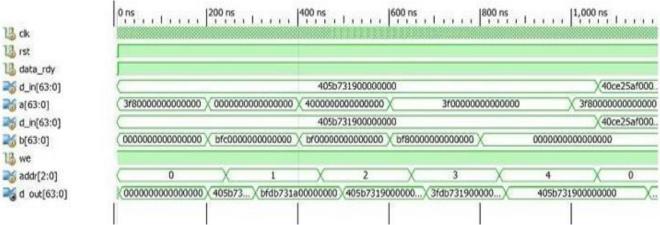


Fig. 4.Simulation results of second order variable fractional delay filter



Design of Variable Fractional Delay Filter using FIR Filter Approximation

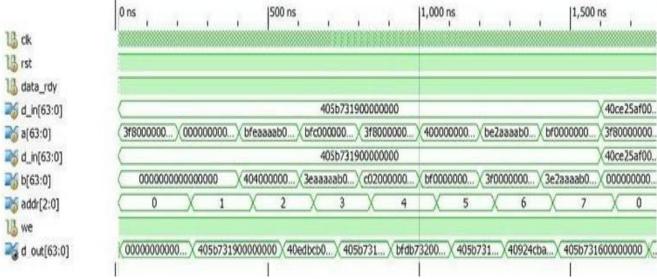


Fig. 5.Simulation results of third order variable fractional delay filter

The simulation results of the variable fractional delay filter using FIR filter are shown in Fig. 3, Fig. 4 and Fig. 5.

(i) First order variable fractional delay filter result:

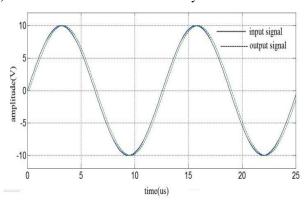


Fig. 6.Simulation result of a first order variable fractional delay filter

The time delay difference between the input signals to output signal is equal to 164 nsec.

(ii)Second order variable fractional delay filter result:

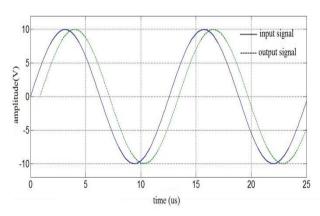


Fig. 7.Simulation result of a second order variable fractional delay filter

The time delay difference between the input signals to output signal is equal to 857 nsec.

(iii)third order variable fractional delay filter result:

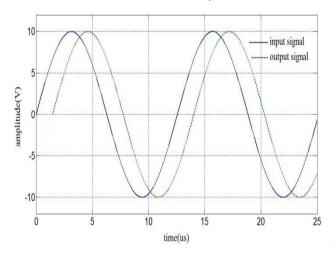


Fig. 8.Simulation result of a third order variable fractional delay filter

The time delay difference between the input signals to output signal is equal to 1457 nsec.

The below Table- I shows the time delay difference between the input signal and output signal of variable fractional delay filter from zero to fifth order filter.

Table- I						
	first order	second order	third order	fourth order	fifth order	
time (ns) delay(ns)	164	857	1457	2671	3560	





Selected Device: 7k325tffg900-2

Slice Logic Utilization:

 Number of Slice Registers:
 11810 out of 407600
 2%

 Number of Slice LUTs:
 15679 out of 203800
 7%

 Number used as Logic:
 15595 out of 203800
 7%

 Number used as Memory:
 84 out of 64000
 0%

 Number used as SRL:
 84

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 19111

Number with an unused Flip Flop: 7301 out of 19111 38%

Number with an unused LUT: 3432 out of 19111 17%

Number of fully used LUT-FF pairs: 8378 out of 19111 43%

Number of unique control sets: 143

IO Utilization:

Number of IOs: 263

Number of bonded IOBs: 263 out of 500 52%

Specific Feature Utilization:

Number of BUFG/BUFGCTRLs: 1 out of 32 3%

Timing Summary:

Speed Grade: -2

Minimum period: 2.758ns (Maximum Frequency: 362.608MHz)

Minimum input arrival time before clock: 1.288ns

Maximum output required time after clock: 0.575ns

Fig. 9.Device Utilization summary

The variable fractional delay filter is designed and simulation results are shown in Fig.3-8. Fig. 9 shows the device utilization summary. In this paper variable fractional delay filer designed from first order to fifth order. If the order of the filter increases, the number of FIR filters in VFD filters also increases. In the design due to the use of more number of FIR filters, number of multipliers and number of adders increases. If the number of operations increases, delay also increases. Periodic signal is taken as an input to the variable fractional delay filter. The delayed output is taken as a result.

In the first order variable fractional delay filter have only two FIR filters, this two are connect in cascade form. The delay difference between input and out of first order variable fractional delay filter is shown in Fig. 6. i.e 164 nsec. In the second order variable fractional delay filter have three FIR filters .this three are connect in cascade form.

The delay difference between input and out of first order variable fractional delay filter is shown in Fig. 7.i.e 857 nsec. Similarly, the order of the filter increases number of FIR filter and order of the FIR filter increases. If the fractional delay filters of order N, number of FIR filters is equal to N+1.

V. CONCLUSION

Signal processing application and technical indicator receive the broadband signal by using narrow band beamforming signals. Mainly in broadband system, a digital antenna is used with the disadvantage of pattern distortion, pointing deviation and sidelobe raise.

To avoid these kinds of problems, efficient and reliable realization techniques are used in Beamforming. Digital Fractional Delay is calculated by using Variable Fractional filter to obtain different delays for different order.

Variable fractional delay filter is calculated by two different phase signals from digital antennas and those two different phase signals are converted to in-phase and added together to form a beam forming.

As the order of the filter increases, the delay also increases. In this paper, the delays are calculated and compared from first order to fifth order of variable fractional delay by using software Xilinx version 14.3. More delay (nanoseconds) can be generated by designing higher order variable fractional filters in future.

REFERENCES

- Ming Guo ,Xiaofeng Ma, Shurui Zhang ,Weixing sheng ,"The FPGA Implementation and Variable Fractional Delay Broadband Beamforming,"978-1-4673-8194-9/16,2016.
- Hai Huyen Dam, "Design of Variable Fractional Delay Filter with Fractional Delay Constraints," IEEE Signal Processing letters, vol. 21, no. 11, November 2014.
- Jong-Jy Shyu, Soo-Chang Pei, "A generalized approach to the design of variable fractional-delay FIR digital filters," Signal Processing 88 (2008) 1428–1435.
- Çagatay Candan, "An Efficient Filtering Structure for Lagrange Interpolation," IEEE signal processing letters, vol. 14, no. 1, January 2007.
- Tian-Bo Deng, "Symmetry-Based Low-Complexity Variable Fractional- Delay FIR Filters," IEEE International Symposium on Communications and Information Technologies, 2004, 194-199.
- T.-B. Deng, "Discretization-free design of variable fractional-delay FIR digital filters," IEEE Trans. Circuits Syf. 11, vol. 48, pp. 637-644, June 2001
- A. Tarczynski, G.D. Cain, E. Hermowicz, and M. Rojewski. "WLS design of variable frequency response FIR filters," Proc. IEEE ISCAS'97, pp. 2244.2247, Hong Kong. June 9-12, 1997.
- N. P. Murphy, A. Krukow ski, and I. Kale, "Implementation of a wideband integer and fractional delay element," Electronics letters, vol. 30, no.20, pp. 1658-1659, Sep. 1994.
- R. Zarour and M. M. Fahmy, "A Design technique for variable digital filters," IEEE Trans. Circuits Syst., vol. 36. pp. 1473-1478, Nov. 1989.
- C. W. Farrow, "A continuously variable digital delay element," Pmc. IEEE ISCAS'88, vol. 3, pp. 2641-2645, Espoo, Finland, June 6-9, 1988.

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