SILICON MIGRATION OF THROUGH-HOLES IN SINGLE- AND POLY-CRYSTALLINE SILICON MEMBRANES

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ABSTRACT

In this work we present migration phenomenon of through-holes in silicon membranes. The sealing of through-holes in hydrogen ambient at high temperature (1130°C) with various dimensions and annealing time durations was investigated in both single-crystalline silicon (sc-Si) and poly-crystalline silicon (poly-Si) membranes. The sealing process in silicon was observed as highly dependent on local crystal grain geometry, leading to more distributed, unpredictable migration rates and shape evolutions in poly-Si compared to holes in sc-Si. These findings can be leveraged in fabrication processes that require a balance between silicon migration and deposition.

INTRODUCTION

Silicon migration is a mass transportation effect that occurs even below the melting point of silicon. This effect is well-documented for single-crystalline silicon (sc-Si) by various groups at high temperatures and low-pressure deoxidizing ambient such as hydrogen (H_2) and at ultra high vacuum (UHV) [1,2]. The atomic-level smoothening of silicon transforms small features to minimize the surface energy [1,3,4]. Silicon migration is already utilized in instances such as the "silicon-on-nothing" developed by Mizushima et al [5].

The "epi-seal encapsulation" process developed by Robert Bosch GmbH and Stanford University, which utilizes epitaxially deposited silicon as the released membrane, has demonstrated promising results in diverse MEMS products such as resonators [6] and pressure sensors [7]. This process utilizes poly-crystalline silicon (poly-Si) membranes which function as encapsulation for resonators/inertial sensors and a diaphragm for pressure sensors. The membranes are patterned with through-holes and after removing silicon dioxide (SiO_2) with vapor-phase hydrofluoric acid (vHF), epitaxial poly-Si deposition is employed to seal these holes. This sealing deposition is conducted at a very high temperature (>1000°C) in hydrogen ambient, and as a by-product, silicon migration occurs around the through-holes.

The effect of release-hole migration during this sealing deposition can be an important factor for the sensor performance. For example, in case of pressure sensor applications, if these through-holes are not sealed at the bottom of the membrane, which is often the case of typical non-conformal deposition-based sealing, it makes the membrane softer, resulting in unpredictable sensitivity. In the case of inertial sensors, the topography in out-of-plane electrodes can become the source of noise during the in-plane movement. For such reasons, the effect of silicon migration on through-holes in the epitaxially deposited silicon membrane has to be further investigated and controlled.

Though the phenomenon of silicon migration of through-hole geometries in membranes has been preliminarily explored in previous works [5,3], these past studies limited their scope to only sc-Si and a few through-hole geometries. Therefore more research needs to be done to make it rather applicable for real MEMS device fabrication. Consequently this work extends our previous studies for better understanding with the following three primary focuses: 1) expansion to poly-Si for the comparison of migration behavior in sc-Si and poly-Si, 2) diverse through-hole geometries to investigate the effects of size/shape differences of etched through-holes, and 3) time-dependence evolution of the hole geometry migration aiming at three-dimensional hole geometry engineering.

For such purposes, through-holes with diverse shapes and dimensions were patterned in both sc-Si and poly-Si suspended membranes, and the shape evolution of those through-holes were observed and analyzed using a scanning electron microscope (SEM) after a high temperature anneal in low-pressure H_2 ambient for different time durations. The time dependence of through-hole shapes was also compared with the Matlab-based simulation results from the previous work in [8].

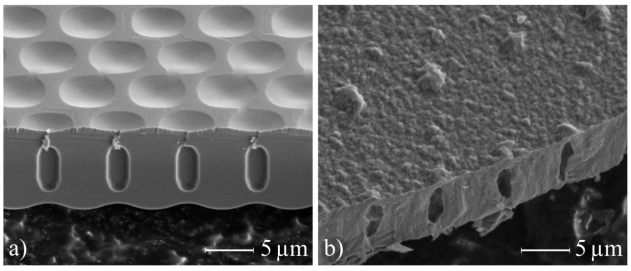

Figure 1: Image of direct comparison of single-crystalline and poly-crystalline through-holes after 10,000 s of annealing in hydrogen ambient

FABRICATION

Since most previous work on this topic was performed on sc-Si, two sets of samples were fabricated. This allowed comparison of the results to previous studies as well as a direct comparison between sc-Si and poly-Si (Figure 1).

Figure 2 shows the schematics of the fabricated devices. For the single-crystalline variant commercially produced 100 mm silicon-on-insulator (SOI) wafers were used with a 2-µm-thick buried silicon oxide (BOX) and a 10-µm-thick device layer with (100) orientation (p-type boron doped, 1-2 mΩcm). For the poly-crystalline samples, the process started on 100 mm silicon wafers (100) with a resistivity of 10-20 Ωcm, also p-type doped with boron. These wafers were then processed to become "poly silicon-on-insulator" (PSOI) wafers (Figure 2 a*) as a comparable starting point to the SOI wafers. Therefore a 2-µm-thick silicon dioxide (SiO_2) layer was thermally grown at 1000°C, followed by epitaxial deposition of a 12-µm-thick boron doped (p-type) poly-Si layer. The poly-Si deposition was performed in a reduced-pressure epitaxial reactor by Applied Materials (Centura EPI). The 12 µm of poly-Si were deposited in steps of 3 µm due to the tool limitations, including a seed layer before the first step. For the seed layer deposition, which is negligibly thin compared to the total thickness, silane (SiH_4) with H_2 as carrier was used as a precursor at 800°C and 600 Torr with a gas flow of 60 sccm for 90 s. For each 3 µm poly-Si deposition step the precursor was Dichlorosilane (DCS, SiH_2Cl_2) at 1080°C and 30 Torr with flow rate of 400 sccm in a H_2 carrier for 196 s; p-type dopant (1% diborane, B_2H_6) was simulta-

neously flowed at 100 sccm. After the deposition the thickness was reduced to 10 µm and the surface was smoothened by chemical mechanical polishing (CMP). At this point the PSOI wafers had comparable properties to the chosen SOI wafers and therefore the following processing steps could be performed on both variants in parallel (Figure 2 a1/b1).

With optical lithography the wafers were patterned (Figure 3 and Table 1) and the device layer etched utilizing deep reactive ion etching (DRIE) to get high aspect ratio through-holes (Figure 2 a2/b2). Table 1 shows the different shapes and dimensions of the various structures. Due to constraints in lithography and etching 0.8 µm was chosen on the lower end as the limiting dimension. This width is constant for variants V2, V3, V6, and as diameter for V1. The length of each was varied from 0.8 µm to 5 µm. V4 and V5 have the same area as V2 but a different aspect ratio and therefore the width is wider than the limiting dimension. The through-holes were arranged in two patterns: One is rectangular, where all holes are equally distanced, and the other a circular one with alternating through-hole density due to the radial arrangement (Figure 3d). The circular version is used for a membrane in an actual device design by this group [7].

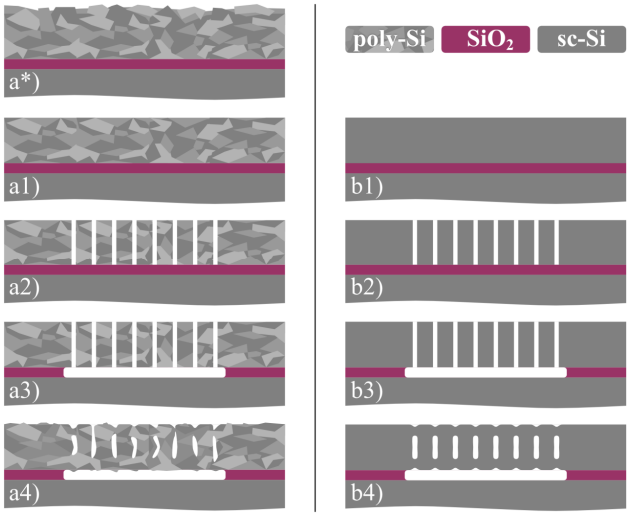

Figure 2: Process flow for a) poly-Si and b) sc-Si wafers. a) thermal SiO_2 grown on Si wafer and deposition of poly-Si in epitaxial reactor; a1) CMP to smoothen the surface; a2) through-hole patterning with DRIE a3) vHF etching to release membrane a4) annealing in H_2 ambient b1) SOI wafer b2) through-hole patterning with DRIE b3) vHF etching to release membrane b4) annealing in H_2 ambient*

Table 1: Overview of through-hole shape variations. These shapes were patterned using deep reactive ion etching (DRIE) through the 10-µm silicon device layer. The hole coverage is regarding to the rectangular membrane.

	V1	V2	V3	V4	V5	V6
Shape	●	▬	▮	■	▬	▬
	circular	rectangular	rect.	rect.	rect.	rect.
Dimensions	Ø 0.8 µm	0.8 µm × 5 µm	0.8 µm × 0.8 µm	2 µm × 2 µm	1.4 µm × 2.86 µm	0.8 µm × 2.5 µm
Area	0.503 µm²	4 µm²	0.64 µm²	4 µm²	4 µm²	2 µm²
Hole coverage	1.7 %	7.4 %	2.1 %	9.5 %	9.5 %	4.7 %

The underlying oxide was removed by vHF etching after reducing the moisture with a rapid thermal annealing (RTA) step (Figure 2 a3/b3). To confirm that the membranes are completely released, the samples were inspected with an infrared microscope.

The wafers were subsequently annealed in the epi process chamber (Figure 2 a4/b4) for varying time durations at 1130°C and 20 Torr in a H_2 ambient. For the poly-crystalline wafers the annealing time durations were chosen as 0 s (no annealing), 1000 s, 2000 s, 3000 s, 4000 s, and 10000 s and for the SOI wafers 0 s, 2000 s, 4000 s, and 10000 s.

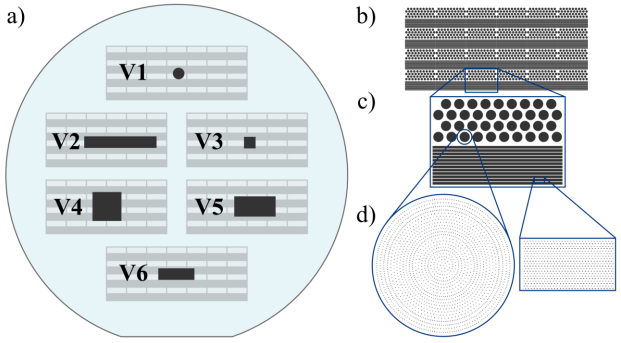

Figure 3: Mask layout for the through-holes a) arrangement on wafer of the various through-holes regions b) arrangement of the reticles for each through-hole variant, high number of repetition to raise chances for successful cleaving c) reticle layout d) left: circular membrane; right: rectangular membrane

CHARACTERIZATION AND DISCUSSION

The characterization was done on an SEM. Top-surface, bottom-surface, and cross-section images were taken of the membrane. For the cross-section images samples were mechanically cleaved. For the bottom-surface view of the membrane double coated conductive tabs were used; by attaching the tabs to the top surface and quickly removing, membranes were ripped out-of-plane, revealing the bottom side.

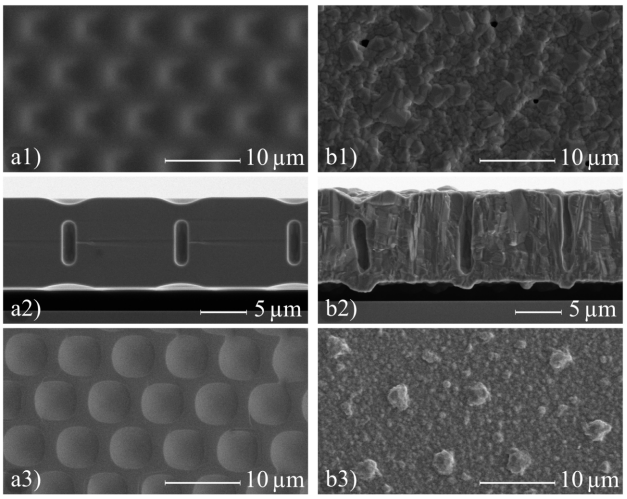

Figure 4: SEM images of sc-Si and poly-Si V6 through-holes after 10000 s of annealing. a1) sc-Si top view a2) sc-Si cross section a3) sc-Si bottom view b1) poly-Si top view b2) poly-Si cross section b3) poly-Si bottom view

These results are qualitatively consistent with the results from a silicon migration model developed by Kant [8] based on Mullins surface diffusion equation for sc-Si. Simulations with the same through-hole dimensions and similar conditions (temperature, pressure, ambient) were performed and are shown in Figure 5. The displayed progression towards closure can be compared with the cross-section shown in Figure 6.

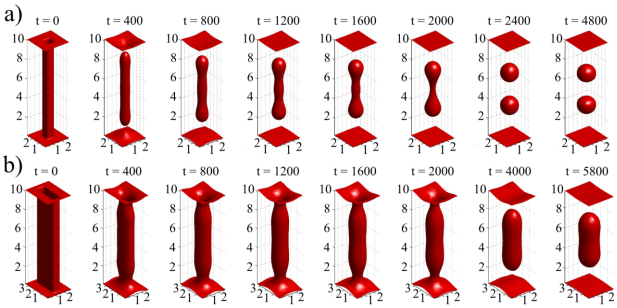

Figure 5: Simulation V3 based on Mullins surface diffusion equation (time units do not correspond to seconds)
a) V3 through hole b) V6 through-hole

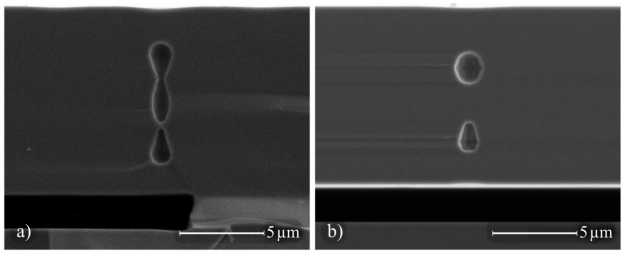

Figure 6: Cross section of single crystal Si V1 through-hole a) after 2,000 s b) after 10,000 s

The thickness of the membrane for SOI wafers stays approximately the same (measured to be about 9.9-10.1 µm for sc-Si after 10,000 s of annealing). A reduction in thickness due to volume conservation like witnessed by Provine et al [9] was not observed nor expected to be significant enough to notice. The volume of the through-holes is too small in relation to the pitch, so that the coverage of the through-holes is in the range of 1-10 % (Table 1).

Another finding in poly-Si is a clear distinction between the upper and the lower side of the membrane; nearly all patterned through-holes were closed on the bottom side after the 10,000 s anneal, while some holes remain open on the top side (Figure 4b). Additionally, the migration sealing of poly-Si through holes left 'lids' that grew out-of-plane (Figure 4b2), in contrast to the indented trench closures on the top side and in sc-Si samples shown in Figure 4a. This can be explained by the vertically oriented grain size gradient in the poly-Si membrane, which was also observed by Ng et al [10] using a similar fabrication process. The grain size increases from the base (~200 nm) towards the top (~3 µm). Therefore the diffusion mobility is higher at the bottom side leading to more active migration.

Figure 7 shows the evolution of the top-side openings for a) sc-Si and b) poly-Si. In Figure 7a3) the cross-section of the simulated V6 through-hole (0.8 µm x 2.5 µm) over 1000 time units is plotted. The qualitative transformation of the simulation correlates with the measured results. Both sc-Si and poly-Si morph from an elongated rectangular shape to a circular footprint. In the single-crystalline case the result is an almost perfect circle, for the poly-Si the trend towards a circular shape is clearly visible although it is more non-uniform (Figure 7b3).

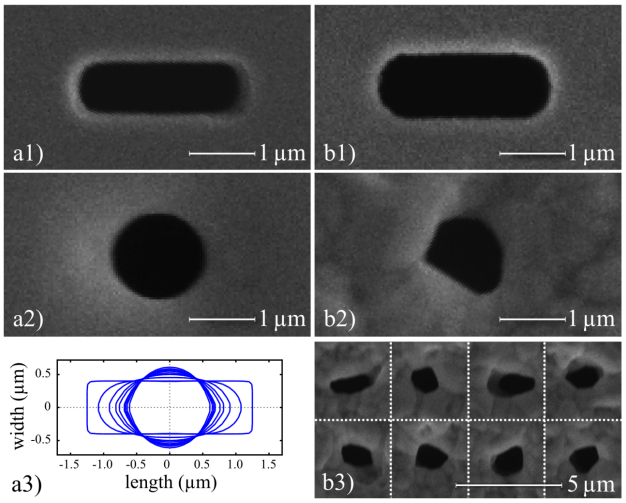

Figure 7: Transformation of a) sc-Si and b) poly-Si V6 through-holes from no annealing (a1,b1) to 2000 s (a2,b2/3). a3) shows the predicted evolution by the simulation for 1000 time units.

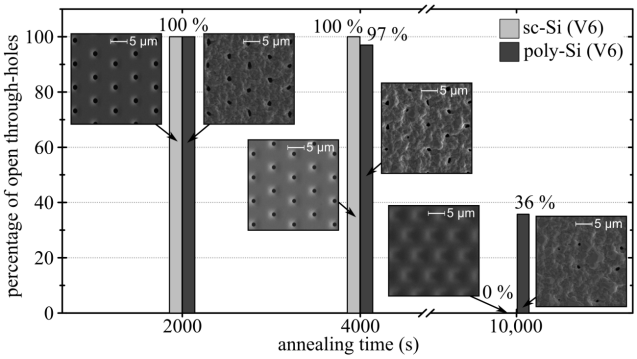

Figure 8: Comparison of V6 through-holes grown closed between sc-Si and poly-Si. All holes in sc-Si were in virtually the same sealing state: all open at 4,000 s and all closed at 10,000 s. In contrast, holes in poly-Si evolve gradually towards closure: some are already closed after 4,000 s while a few are still open even after 10,000s

Figure 8 compares the top side of the V6 membranes for sc-Si and poly-Si. Note that holes in sc-Si migrate at the same pace: all open at 4,000 s and all closed at 10,000 s. In contrast, through-holes in poly-Si evolve gradually towards closure; some are already closed after 4,000 s while a few still remain open even after 10,000 s indicating a high degree of non-uniformity across the device and the wafer.

The dependency of the through-hole orientation is displayed in Figure 9. In the case of sc-Si, there is an influence in the hole-sealing behavior clearly visible after 2,000 s and 4,000 s, but after 10,000 s all holes appear circular. This is explainable by the crystal orientation in the SOI wafers and the dependency of the migration rates on crystal orientation [8]. After a certain time changes in shape become slower (see Figure 5), and the differences in migration rate consequently even out. For the poly-Si samples the variation between through-holes has no correlation to the orientation on the wafer, since there is no global crystal orientation, and therefore the migration process is more non-uniform.

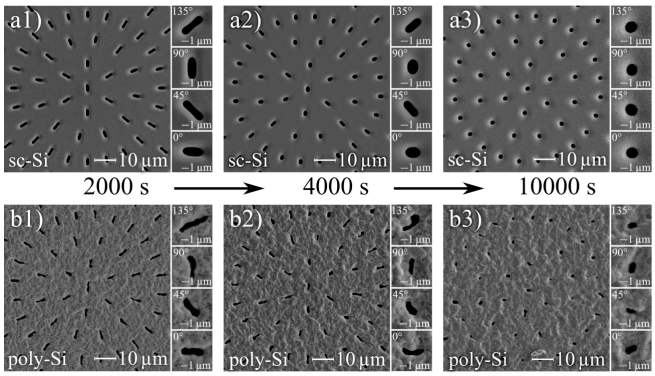

Figure 9: Top view SEM comparing the influence of crystal orientation on the example of through-hole V2; a) sc-Si; b) poly-Si. In the case of sc-Si, the crystal orientation dependence is clearly visible until 2,000-4,000 s, whereas holes in poly-Si migrate more non-uniformly.

CONCLUSION

The analysis of the samples and comparison with previous studies shows, that despite of the similarities, there are major differences in the evolution of the through-holes and the surface topology between sc-Si and poly-Si. Whereas the through-holes in sc-Si are generally uniform and homogeneous all over the membrane respectively the wafer, each through-hole in poly-Si evolves differently. The uniform behavior of the sc-Si makes the annealing process a reliable method for sealing, since after a specific time period all through-holes are closed. Migration of through-holes in poly-Si on the other hand is less predictable and gradual. While some holes are closed even earlier than in sc-Si, others take significantly longer than the average portion of the through-holes. It is more of a statistical process, which leaves the possibility of unclosed through-holes. Because a single open hole will compromise the hermeticity of the encapsulation, the exclusive use of migration in poly-Si is not an acceptable encapsulation technique on its own.

Also within the scope of a single through-hole, there are significant differences between the upper and lower side of the membrane, in contrast to the fairly symmetrical migration process in sc-Si. The bottom and top side of the closed off through-holes in the membrane are in the sc-Si scenario indented. In the case of poly-Si the vertical gradient in silicon grain size causes indented or quasi plane top surfaces but "out-of-plane lids" on the bottom side of the membrane.

In addition, there is a dependency in shape evolution visible for sc-Si. Due to the fact that there is no global crystal orientation in a poly-Si membrane, there is no such orientation dependent pattern noticeable.

Unlike the sealing with conformal deposition, the migration process is highly dependent on the through-hole geometry. For deposition, either the width or the length, the shorter one determines the critical dimension to seal the through-holes, which is not the case for migration sealing which depends more on the overall geometry such as shape, area, and perimeter of through holes. On the other hand it is difficult to seal the through-hole from bottom to top simultaneously with deposition methods, therefore insufficient sealing on the bottom side is usually observed.

To prevent the risk of possible unsealed release-holes and to minimize the annealing time, but also accomplish a satisfactory plane lower membrane side, a hybrid of migration sealing and deposition is proposed. The outcome of this study enables further investigation to find optimum release-hole geometry for poly-Si and is directly applicable to release-hole sealing in silicon film encapsulation technology such as "epi-seal encapsulation". It can be also directly applicable to other MEMS device fabrication such as micro-fluidic channels for lab-on-a-chips or chip coolers.

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