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A SCALABLE NOC IMPLEMENTATIONS OF A POWER EFFICIENT ROUTER DESIGN

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ABSTRACT

The most promising technology for future multi-core computers is Wireless Networks-on-Chip (WNoC) because they are capable of overcoming the limitations of conventional Networks-on-Chip (NoCs). Numerous benefits of NoCs with WI have been demonstrated through in-depth analyses. Hardware and routers that are connected to WI generally consume relatively large amounts of static power. Situations where most devices are idle for long periods of time, it is a smart idea to turn off individual routers to reduce total power consumption. WNOCs with broadcast-capable antennas are also limited to only one active wireless connection, and many WIs are inactive for long periods. Therefore, we offer a fine-grained router architecture (FGRA) that consumes less power. A power-gated transceiver, which is activated by the receiving antenna whenever a signal is received, further reduces wake-up latency. NBBCs sidestep power-gated routers, alleviating routing delay and congestion further. The buffers also consume a high amount of power dynamically and their power consumption increases rapidly with increasing packet flow rates. Dynamically and statically, the Easy Pass Router reduces power consumption significantly. This proposed architecture improves NoCs in terms of both energy efficiency and performance. In periods of low traffic, switching mechanisms could be used instead of complex pipelined routers to save energy.

I. INTRODUCTION

How long did Moore's law predict that time frame all those years ago, when computers were first developed? The law has proven to be highly valuable in guiding long-term planning and setting R&D goals in the semiconductor industry thanks to his foresight. Matching systems comprise a single chip that includes the processor cores and any other components relevant to the attributes (IPs). In Figure 1, we can see one type of SoC. An IP could consist of a microprocessor, a data memory, a multimedia decoder, and a generic peripheral. Communication between SoCs is centered around the bus. It has been found that traditional bus-centric communication systems suffer from problems such as inefficient bandwidth use, high latency, in capacity to change, and excessive resource consumption.

II. REVIEW OF LITERATURE

[1] L. Chen and T. Pinkston, "NoRD: Node-router decoupling to enable effective power-gating for on-chip routers". Using Node-Router Decoupling (or NoRD), a novel power-aware on-chip network technology, we propose a method for eliminating the dependency between packet-transfer capabilities and router power availability.

[2] An Adaptive Deflection Router with Dual Injection and Ejection Units for Mesh NoCs" by John Jose and Abhijit Das. It is proposed in this study that a new kind of adaptive deflection router should be developed with separate data injection and expelling units. Using a pair of injection units and scattering side buffers, this router makes dynamic routing choices.

[3] A Network-on-Chip Router Elastic Buffer Architecture ElastiStore offers a new, lighter, and faster lightweight elastic buffer architecture that reduces buffering demands without compromising performance. Previous Elastic Buffer (EB) designs are extended to support multiple Virtual Channels (VC).

[4] A network of chip router can provide dynamic virtual channels and index-based arbitration, according to Masoud Oveis-Gharan and Gul N. Khan. It eliminates the problem associated with NoC arbitration by eliminating it. 2Dmesh NoC router was designed and implemented in System-Verilog by the authors.

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[5] Microarchitecture approaches for power gating of execution units, by Z. Xie, Z. Hu, Venerabhadran Zyuban, H. Jacobson, and Pankaj Bose. In this study, the authors investigated a technique such as powergating of execution units to limit leakage.

[6] Specifically, "An ultrafine-grained power-gating technique for routers based on microprocessors for SMPs" by H. Hasegawa, M. Koibuchi, D. Ikebuchi, K. Usami, H. Nakamura, and H. Amano. This technique allows you to control the power delivered to individual router components (such as VC queues, crossbar MUXs, and output latches) at runtime is presented in this study.

[7] J. Y. Zhao, F. Ge, J. Ouyang, D. Zhang, and Y. Xie in "DimNoC: A Dim silicon approach towards power-efficient on-chip networks" As part of their DimNoC solution, the authors propose sleepy SRAM and STT-RAM technology as a means of overcoming the dark silicon problems inherent in Network-on-Chip (NoC).

[8] R. The authors of this paper present Panthre, a technique that enables selected devices to sleep uninterrupted for extended periods by using powergating, in order to address the problem of NoC power consumption.

III. IDENTIFICATION OF PROBLEMS

A few years from now, integrated systems will integrate hundreds of IP cores, equivalent to hundreds of billions of transistors. In order to provide rich multimedia and networking services, IP cores must be powerful enough to run a wide range of networking and multimedia applications. Through the use of available resources, these IP cores can work together effectively. As these intricate systems are designed, there are several considerations to take into account. The challenge of creating a reliable connectivity network that enables IP cores to be linked on-chip is challenging. Another challenge is mapping applications so they can take full advantage of the hardware resources. It is essential to implement novel implementations in order to design Network-on-Chip (NoC) architectures that provide high throughput and low-latency. The router's buffer architecture has an impact on network performance and implementation details.

IV. OUR PROPOSED SOLUTION

We present an alternative design for the Easy Pass Router in this work. It saves a lot of static power by eliminating wake-up latency overheads. A regular router is used during peak traffic times, and a switch is used during off-peak and low-traffic periods. As a consequence, incoming packets can be routed by the router without having to wake it from its sleep state completely. The EZ-Pass switch is a bypass circuit that consists of MUXs, deMUXs, and single-flit latches (DEMUXs).

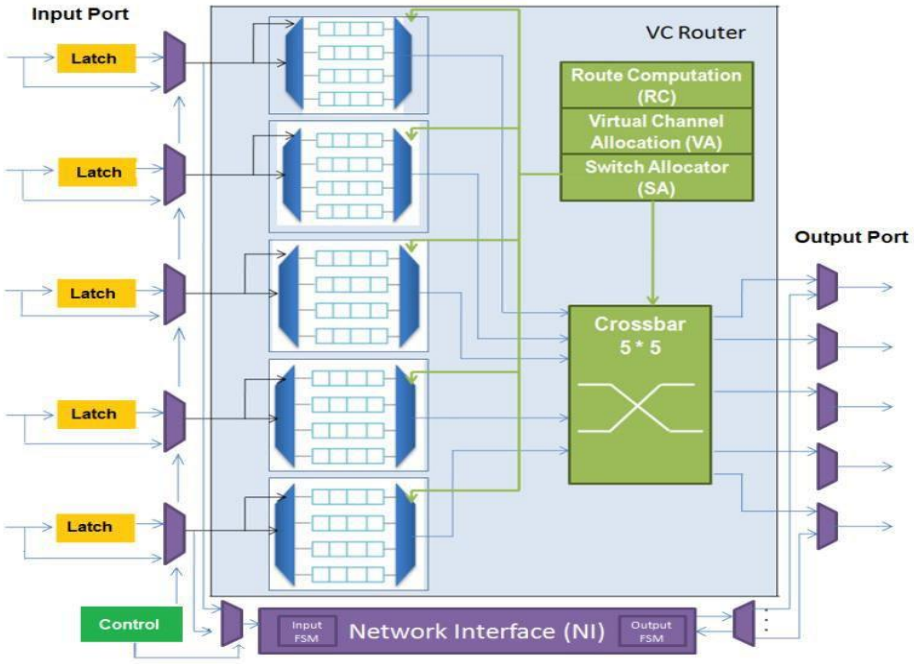

Figure 1: Proposed EZ Pass router Architecture

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V. PROPOSED METHODOLOGY

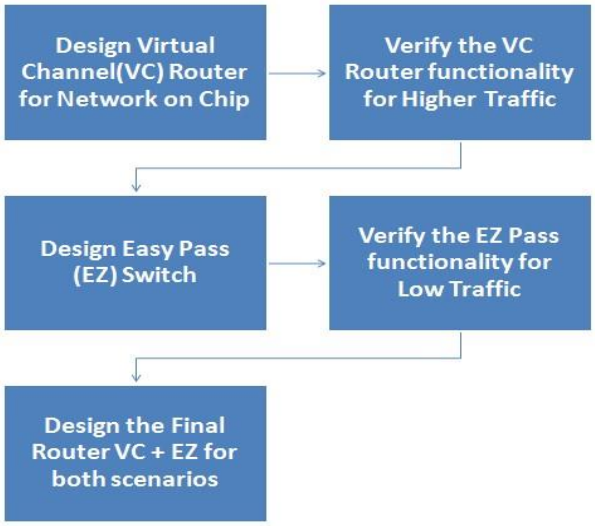

Figure 2: Proposed methodology

5.1. Architecture of virtual channels:

By cutting a physical channel into smaller pieces, a virtual channel is created. By providing multiple entry points into the network, virtual channels alleviate congestion caused by a large number of flows competing for the same one.

5.2. The virtual channel allocation algorithm

Physical channels are shared among the router's many requestor input ports. If more than one requester wants to share the same physical channel, an arbitrator would be helpful.

5.3. Switches for allocating resources

Each input and output port along a route is assigned a single virtual channel once a route is designated as a routing path. Standard routers have other virtual circuits (VCs) which they use for other functions. The packets are separated by virtual channels for that reason.

5.4. Switches and crossbars

Upon scheduling the fabric module, the input and output ports are physically connected when the scheduler approves. By using the module's CNTRL input, you can adjust all of the nodes where the crossbars intersect. CNTRL bits associated with crossed points are high if they are high. The crossbar fabric demonstrates the benefits of a NoC router.

5.5. Quick passage is enabled by input latches on the EZ Pass Switch.

Input ports North, South, East, West, and local of the EZ Pass Switch are equipped with one-flit-latches. VC Routers are equipped with input latches that prevent flits from being lost when the computer is turned off. Through latches or straight flits, the EZ Pass Switch Control Unit transmits control signals to the network interface.

5.6. The control unit for the EZ Pass switch is partially hidden

Data transmission outside of the NI is regulated by three primary signals from the EZ Pass Control unit. Input port MUXs receive a control sel IP signal from the VC Router for picking flits from latches or directly; the output port DMUXs receive a control sel op signal from the VC Router or the NI for selecting the winning flits; and the VC Router receives a control sel NI signal for selecting the NI.

5.7. Interfaces for networks

The NI processes incoming flits through the EZ Pass route when a router is disabled and an incoming flit is detected. A FSM is included in both the input and output architecture to handle flits. Input FSMs receive NI control signals from EZ Pass Switch Control Units, which send the flit signals of relevant ports directly to the output FSMs. Competition for output ports in the FSM is successful, and the flits are rewarded for their efforts.

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5.8. Connections to output ports

A DMUX is attached to each output port, receiving a control signal from either the VC router or the NI.

VI. RESULTS

Analyses Results:

6.1. The following waveforms are shown in a simulation of an EZ Pass Router:

A low traffic level and a disabled router will not prevent EZ Pass from working. By default, the router is not enabled, but NI sends flits in response to the requests in the input port.

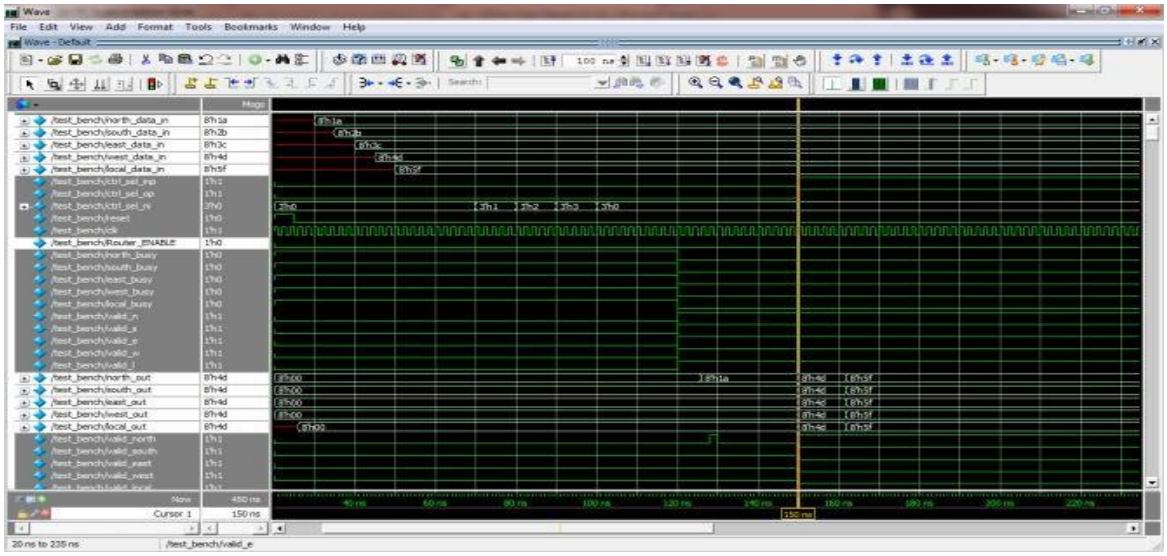

Figure 3: An analysis of the proposed EZ Pass router's simulation waveforms

6.2. A reduction in network traffic in VC routers:

Both light and heavy loads on the network are handled well by the VC Router as demonstrated by the waveforms shown here. A request signal is used in low-traffic conditions to direct flits. When traffic is at its peak, the request will be prioritized and routed accordingly. I will make the case for port accessibility as the highest priority for the sake of argument.

are N, S, E, W, L(low ⊥ high)

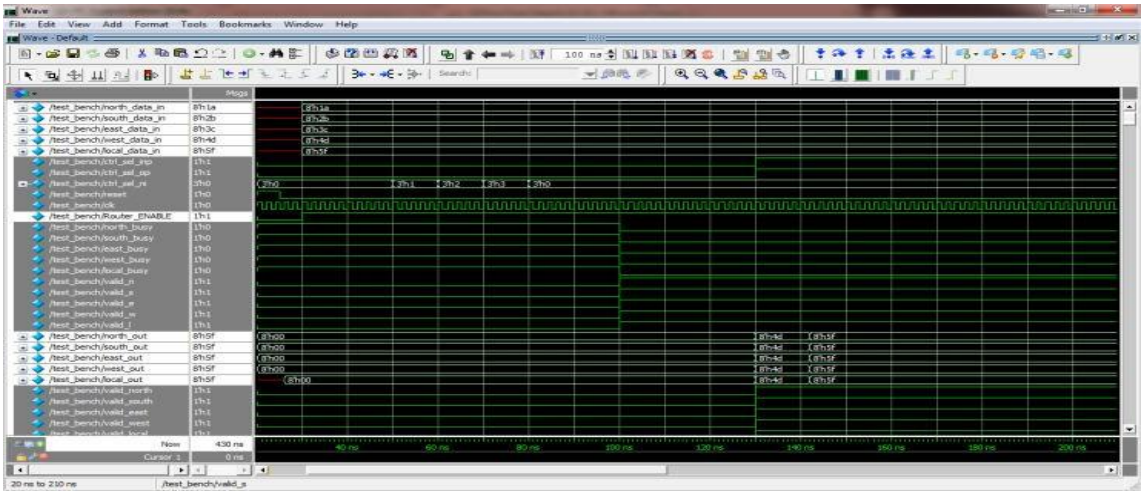

Figure 4: Less traffic on VC routers

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6.3. Network traffic on a VC router:

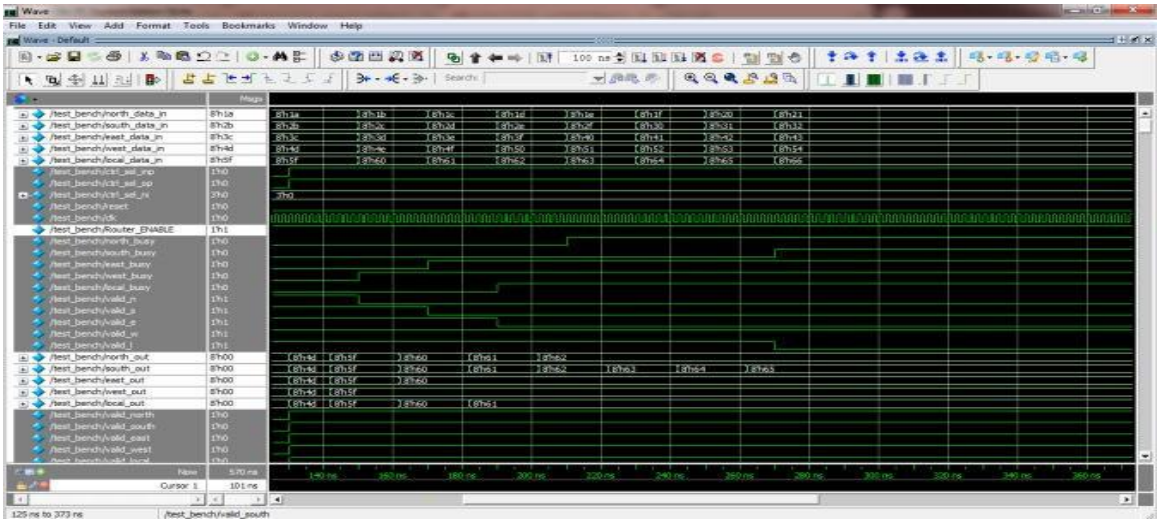

Figure 5: Heavy network traffic on VC routers

6.4. Schematics for EZ Pass Switches

Once the HDL synthesis phase of synthesis is complete, a schematic representation of the synthesised source file is displayed. Using standard components, you can verify and express the optimal design using adders, multipliers, counters, AND gates, and OR gates. In the final product, we fixed problems identified in the RTL schematic below by analyzing it early.

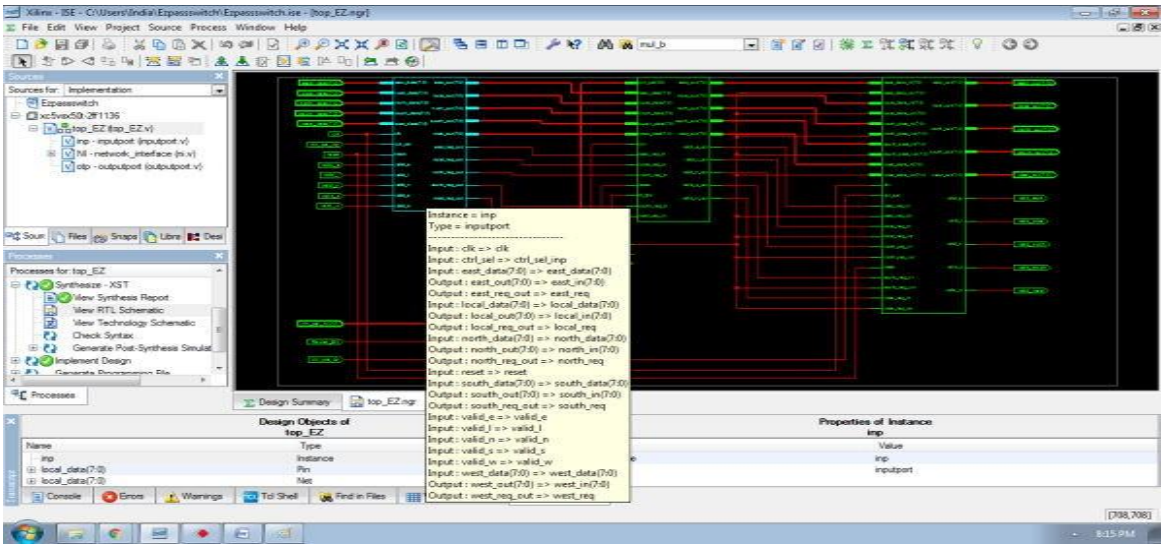

Figure 6: A schematic of the design of the EZ Pass switch in RTL

6.5. Critical evaluation and outcome

Our design and its effectiveness can be evaluated based on the synthesis report. Xilinx ISE and Vivado tools are used at this point to evaluate the parameters of the proposed design.

6.6. An FPGA-based design pipeline, uses EZ Pass Switch number of slices or equivalent gate count for area analysis. After a successful synthesis of our design, we get a Xilinx Device Utilization Summary in which the total number of slices is shown.

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Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slice Registers	247	32640	0%
Number of Slice LUTs	160	32640	0%
Number of fully used LUT-FF pairs	135	272	49%
Number of bonded IOBs	98	480	20%
Number of BUFG/BUFGCTRLs	1	32	3%

Figure 7: Summary of device usage for EZ Pass Switches

6.7. Diagrammatic Synopsis of the EZ Pass Switch's Timing

When using Synthesis, the delay analysis yields the Timing Report. Within its pages, you'll find an analysis of the crucial path and a summary of the bottlenecks in our design. In the complete Synthesis Report, this information is also included. Period of 3.138ns or Less (Frequency Maximum: 318.634MHz)

6.8. Report on power

For the power report, we estimate the real-world dynamic and static power consumption using the Vivado tool and the Atlys FPGA. All voltage rails and supporting circuitry in an FPGA must be powered by leakage power from transistors after configuration. Methods, voltages, and temperatures all affect a device's static power. Static power represents constant-state leakage within a device.

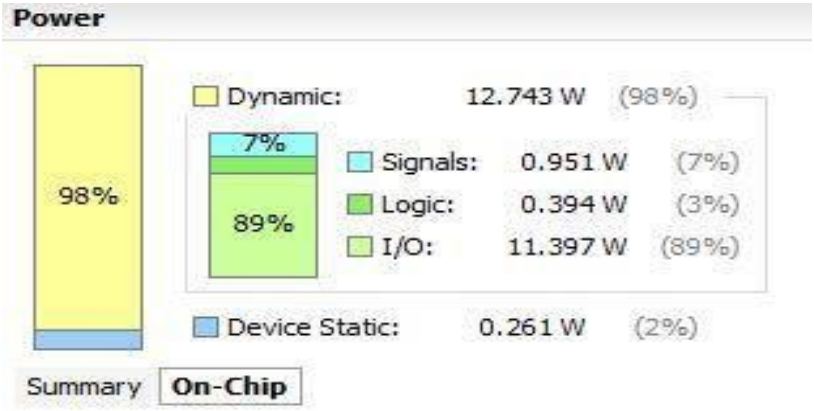

Figure 8: Report on EZ Pass Switch's static & dynamic power

A FPGA's internal power consumption, equal to the sum of Device Static Power and Design Power, is called internal power

Power consumed on chip

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Figure 9: Report on the power consumption of VC routers

6.11. Performance evaluation:

EZ pass switches consume a lot less energy and space than other switch designs. This conclusion can be drawn from the above data and comparisons. A higher frequency is used in the EZ pass switch, ensuring greater efficiency. It has been determined from the timing information provided by both designs that the EZ pass switch has a very low latency and delay time.

VII. CONCLUSION

According to the results of this study, NoC routers can be enhanced to provide enhanced functionality. With this technique, the clock cycles of on-chip routers may be dramatically reduced. Simulated results indicate that performing VC allocation and SA simultaneously will have little to no effect on router performance. There are 1074 flip-flops in this router, which is quite high when compared to other router configurations, but the frequency of the flip-flops is very high, helping to reduce network latency and boost performance. On-chip connection is accelerated and communication capacity is increased using the proposed simple pass router design. The availability of virtual circuit (VC) routers for handling more traffic makes modular network architecture more appealing. The proposed layout makes effective use of the NI module. When traffic is light, it may function as a by-pass switch.

Impacts that may arise in the future

With the increasing complexity of future Networks on Chip, CMP cores will require increased energy consumption. System-on-chips will face significant design and throughput challenges in the future thanks to packet-switched networks. To reduce the VC router's power consumption on the fly, we may switch to a bufferless router architecture or a shared buffer architecture, since buffers are crucial to NoC design. Error correction mechanisms may also be included in Network Interface Modules (NIs). As routing systems evolve, they will need to be resilient, fault-tolerant, and fully adaptable. As an alternative method of designing nanosystems in the future, 3D integrated circuits may be able to be utilized. Based on our understanding of the operation of 3D NoCs and 3D MPSoC processors, we may revise and update our EZ Pass VC Router design.

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